Broadband High Frequency Package Design Using Closed Air-Filled Sealed Cavities

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Abstract

The strict and demanding requirements imposed by both the RF and high-speed digital markets necessitate careful full-wave electromagnetic package modeling and challenging multilayer ceramic manufacturing processes to meet higher bandwidth requirements and better control of signal integrity. In this paper we describe a design methodology using air-filled cavities to provide very broadband electrical performance for leaded ceramic packages. The design methodology utilizes computer simulated time domain reflectometry (TDR) to identify various capacitive and inductive discontinuities associated with the board/package electrical interconnect. Along the signal path, from the printed circuit board to the package, TDR simulations indicate a large capacitive discontinuity near the lead of the package. This capacitive discontinuity limits the frequency bandwidth of the package. The bandwidth can be greatly improved by the introduction of an embedded air-filled cavity inside the package near where the lead is brazed to the package. The air cavity provides an inductive load to the signal path near the capacitive discontinuity, which in effect, allows the signal path to be maintained at a characteristic impedance near 50 ohms. Full-wave modeling and simulation show the marked bandwidth improvement up to 30 GHz, by the introduction of the air-filled sealed cavities.

I. Introduction

The RF microwave and high-speed digital markets require electronic package solutions with increasingly stringent broadband electrical performance requirements. Typical signal bandwidth specifications for the package performance are now in the multi-GHz range. For example, the SONET OC-192 products operate at 10 Gb/s. These digital signals require a package that has low loss up to the third order harmonic (15 GHz). For SONET OC-768 applications, which use a 40 Gb/s digital signal, the third order harmonic is 60 GHz. It is clear that the package can become a bandwidth bottle neck for these high frequency off-chip signals.

The material investigated in this paper for providing a high-frequency bandwidth package solution is 92% alumina used in the high temperature co-fire ceramic (HTCC) multilayer process. HTCC multi-Layer ceramic packaging has been a part of the electronics component industry for decades. This packaging technology was especially dominant in the early microprocessor market because of its inherent hermetic and complex routing capabilities. With the advent of higher frequency Microwave Monolithic Integrated Circuits (MMICs), multi-layer ceramic packages are once again favored for the stable frequency characteristics and typical low loss dielectrics.

In this paper, a full-wave 3D electromagnetic simulator and microwave engineering principles are combined in a design methodology to implement unique structures, such an air cavity [1] and a half-etch lead, which can be built with the current multi-layer processing, to provide broadband high-frequency electronic package solutions to interconnect problems. The design methodology is based on the well-known time domain reflectometry (TDR) method, which the cited references [2-7] offer but a small sample of numerous relevant literature on TDR interconnect modeling. Although the TDR method is very often used in measurements to characterize and model interconnects [8] , the application in this paper of the TDR method is in locating the discontinuities and reducing or eliminating the effects of the discontinuity by introducing a manufacturable physical change in the interconnect structure which electrically compensates for the effects of the first discontinuity.

II. Design Methodology

There are two primary domains in which to characterize and design a broadband electrical interconnect: the frequency and time domain. Each domain provides unique information about the performance of the electrical interconnects. In the frequency domain, the figures of merit for measuring bandwidth performance are the frequency S-parameters, which measure the amount of power reflected and transmitted at an interconnect discontinuity as a function of frequency [9]. In the time domain, the package is characterized by measuring the magnitude of reflections from an input step pulse as a function of time. The reflected pulses can readily be translated to identify the spatial location and a characteristic impedance profile, Z(t), of the interconnect.

Designing in the Frequency Domain

To design a broadband package with a full-wave frequency domain simulation tool, the methodology typically involves taking the electrical interconnect geometry and sectioning the entire electrical interconnect path into smaller models which are judiciously chosen to have 50 ohm impedances at the resulting interfaces of the sections. Each section can then be tuned to minimize insertion loss (S12) and return loss (S22). The sections can then be cascaded together into the full-wave simulator and re-simulated to account for any parasitic coupling possibly omitted from the sectioning process. If the parasitic coupling is weak, there are circuit synthesis methodologies which can take the frequency domain data to create SPICE-compatible circuits ready for analysis. While the methodology is sound, it is often the case that the package geometries are so complicated as to make it impractical or impossible to identify the appropriate sections for modeling. Of course the whole electrical link can be modeled and simulated, but then, because the frequency domain s-parameters do not provide discontinuity information as a function of location, one is left with a combination of applying standard microwave practices and an iterative approach in the design stage. The strong reflective coupling between the multitude of discontinuities makes it nearly impossible to identify which physical features are contributing to limiting the broadband performance.

Designing with Time Domain Reflectometry

The limitation inherent in identifying the location and nature of electrical discontinuities from frequency domain data is removed by the use of time domain reflectometry. The time domain reflectometry method is a well known electrical characterization technique in the microwave measurement community. Using step generators and an oscilloscope, a quasi-step voltage waveform is launched into the electrical signal path of interest. Any discontinuities along the signal path will give rise to reflections. These reflection magnitudes and shapes carry the information as to the precise location and nature (resistive, inductive, or capacitive) of the discontinuities along the line.

The TDR method can also be employed in computer simulations to design broadband packages. The approach taken in this paper is to use the TDR method to make changes to the package before any circuit parameter extraction or circuit synthesis is performed. While the authors recognize the value of incorporating circuit models into analysis that predict interconnect behavior in a system, the intent of using TDR is to guide current manufacturing processes, or identify new processes required to obtain high performance broadband behavior from packages.

III. Full-Wave Electromagnetic Simulations and Design

In Figure 1, a section of a surface mounted leaded package is shown. The electrical interconnect is comprised of a 50 ohm microstrip line on a 10 mil thick printed circuit board (PCB) modeled with a permittivity of 2.94. This microstrip launches a signal to a microstrip line on a ceramic package through a lead interconnect and RF via. The ceramic package is 4 layers, 8 mils thick, mounted unto a heat sink, which in turn is grounded to the ground plane of the PCB. The ground plane for the microstrip return path is 8 mils from the surface of the package. The permittivity of the alumina ceramic is 8.8 and has a frequency dependent loss tangent which varies linearly from approximately .0009 at 1 GHz to .0025 at 40 GHz.

The package and PCB interconnect was modeled in the electromagnetic full-wave simulator Computer Simulation Technology Microwave Studio (CSTMWS), which is a time-domain based tool based on the Finite Integration Theory [10] . In Figure 2, a cross section of Figure 1 is shown. In the course of designing a broadband package, the principle that needs to be applied in order to achieve broadband electrical performance is rather straightforward—the impedance must be controlled along the entire electrical path and must have an input impedance near the desired characteristic impedance of the signal path across any small section much less than the wavelength of the highest frequency of interest. In most microwave applications, this characteristic impedance is 50 ohms.

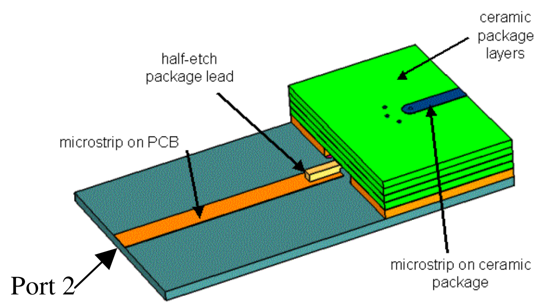

Figure 1. A model of the PCB microstrip to package microstrsip electrical link

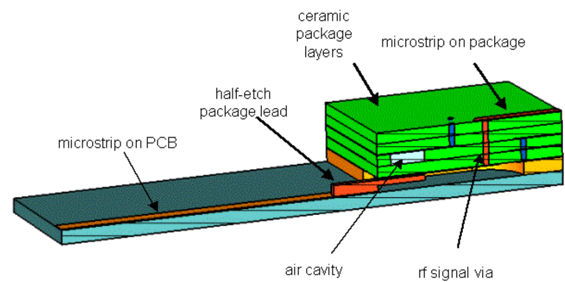

Figure 2. A cross cut of PCB microstrip to package microstrip transition. The lead is a special half-etch and the air cavity is shown.

To control the impedance along the electrical path, the microstrips were designed with 2D quasi-static tools to be 50 Ohms. To find the characteristic impedance for the geometrically complex signal/braze pad and RF via signal path, the CSTMWS TDR simulations are utilized.. There are many degrees of freedom one can choose to reduce the capacitance at this discontinuity, however, a key limitation will be tradeoffs between performance and manufacturability and reliability. With this in mind, there are mechanical reliability concerns if one attempts to control impedance solely by narrowing the braze pad width. Thinking in the third dimension allows the idea of using half-etch lead as shown in Figure 2.

The half-etch signal lead provides an increase in inductance thereby reducing the capacitive discontinuity. The time dependent characteristic impedance for the case where a half etch lead and full lead are shown in Figure 3. Based on standard microwave propagation principles, the velocity of the wave pulse is computed and from this information it is clear that the package board interface is at about 40 picoseconds from the launching port, port 2. As is clear, the half etch lead reduces the capacitive discontinuity. This is indicated by the increase in characteristic impedance of about 4 ohms in this section of the signal path as shown in Figure 3.

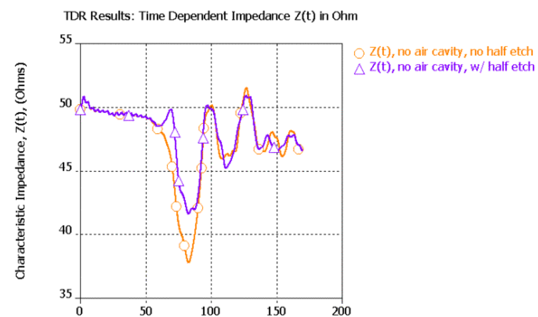

Figure 3. The time dependent characteristic impedance with and without the half-etch lead. No air cavity is in the package

Although the concept of the half-etch lead provides an improvement in the package performance, more improvement is desired however the multilayer manufacturability design rules limits the amount and kind of changes that would be required on the braze pad and lead dimensions. The only degree of freedom left to realistically investigate is the change in the dielectric characteristics of the ceramic material. A change in the effective dielectric constant of the ceramic material can be achieved, in effect, by the introduction of air cavities into the multilayers. This air cavity concept is shown in Figure 2. The air cavity is a small hollow chamber one layer above the layer which has the lead braze pad for lead connections.

In Figure 4, the time dependent characteristic impedance, Z(t), is plotted versus a set of manufacturable air-cavity dimensions. The air-cavity width and thickness is kept constant at .034 in. and .008 in., respectively. The length of the air cavity is varied in the direction of the signal path, .005 in, .015 in, .025 in, and .035 in. As the curves show, we started with a characteristic impedance of about 42

ohms at the lead/braze pad section when no air cavity was present in the package. The characteristic impedance is increased to about 47 with the introduction of the .035 inch long air cavity. It is quite clear that the location of the air-cavity in the layer above the signal lead significantly improves the package performance by bringing the characteristic impedance value close to 50 ohms.

The question now becomes, 'what does the TDR data say about the performance in the frequency domain?" This question is addressed in Figure 5 and Figure 6. In Figure 5, the models were simulated in CSTMWS to generate the frequency domain S-parameters. The return loss, S22, is plotted up to 30 GHz for the air-cavity models discussed thus far. It is evident that the introduction of the air cavities significantly improved the electrical performance of the package in the frequency bandwidth considered. Since bandwidth is defined by specific levels dependent on application, Figure 6 presents the data for improved bandwidth as defined by various return loss levels. For a bandwidth defined by a –10 dB return loss value, the introduction of the air cavities provide modest improvement to the electrical performance of the leaded package. The increase in performance defined by a –25 dB return loss value however is quite dramatic. The bandwidth increases nearly 200%, from about 8 GHz of bandwidth for the no-cavity case to about 23 GHz of bandwidth for the case when the air cavity has a length of .025 inches. Figure 6 also suggests that an optimum length exists for the air-cavity. Except for the bandwidth defined by a –30 dB level, all other bandwidth curves show an optimum bandwidth occurs when the air-cavity length is near .025 inches.

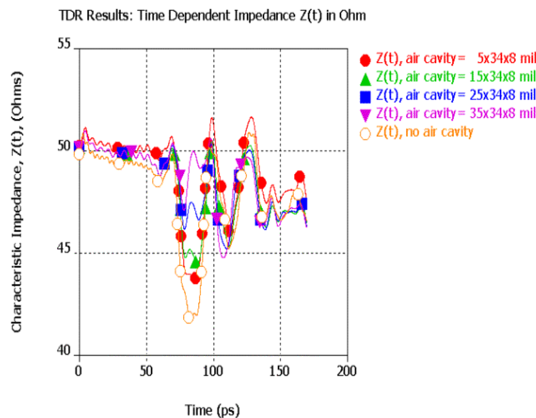

Figure 4. The time dependent characteristic impedance, Z(t) is plotted for a 34 mil wide, 8 mil thick air cavity of various lengths: 5, 15, 25 and 35 mils.

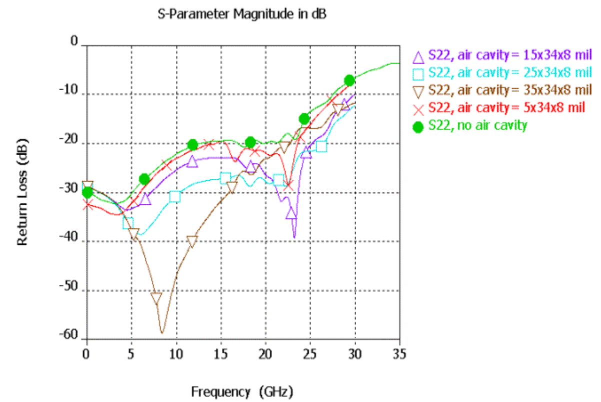

Figure 5. The return loss S-parameter, S22, is plotted for a 34 mil wide, 8 mil thick air cavity of various lengths: 5, 15, 25 and 35 mils.

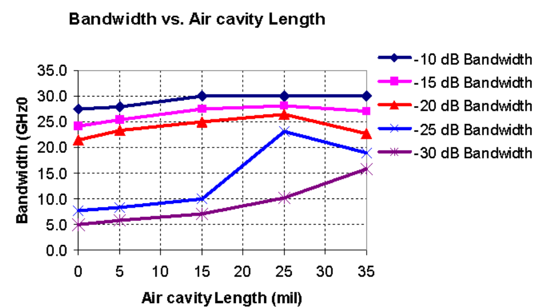

Figure 6. The bandwidth improvement from the use of air cavity is quite evident as the bandwidth is defined with more stringent return loss values.

III. Material and Process Discussion

In this section we briefly discuss the mechanical concerns associated with the introduction of the air-cavity into the HTCC multi-layer process. Several parts were fabricated, cross-sectioned and inspected for delamination. In the initial prototype fabrication phase, the process was standard and without regard to having air cavities in the package substrates.

Figure 7 is a cross section of an air cavity that has no metallization directly above it in any layer interface. As can be seen from the cross section, some delamination has occurred. In Figure 8, delamination can be seen to have occurred in two ceramic layer interfaces directly above the air cavity.

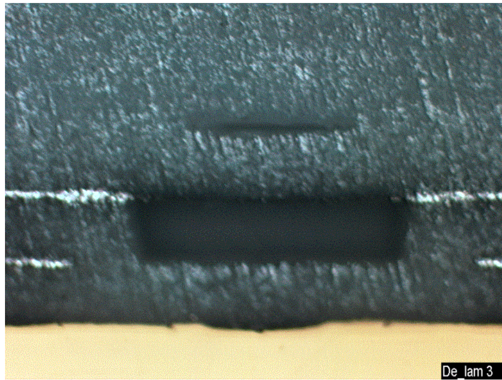

Figure 7. Delamination has occurred directly above the air cavity.

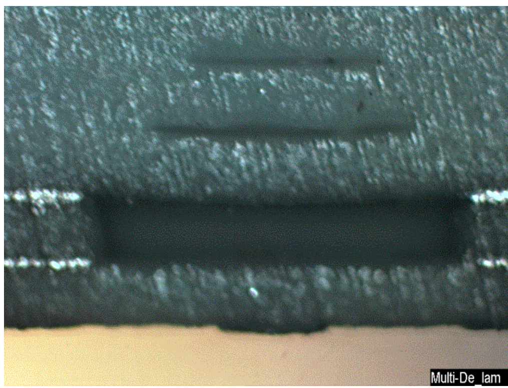

Figure 8. Delamination has occurred in two layers directly above a larger air cavity

In Figure 9, the air cavity is directly under a metal plane. Although no delamination occurred in the first metal plane, delamination did occur in the second metal plane directly above the air cavity. For standard multilayer processing, delamination will occur dependent on the location metal planes and any open cavities above the sealed air cavities. The dependency on delamination and open cavities at the package surface is illustrated in Figure 10. The tested substrates had air cavities in different locations for eventual placement of die. The air cavities in the substrate have locations relative to the open cavities and subsequently underwent different lamination variations. If the multilayer process is slightly changed, delamination can be avoided as shown in Figure 11.

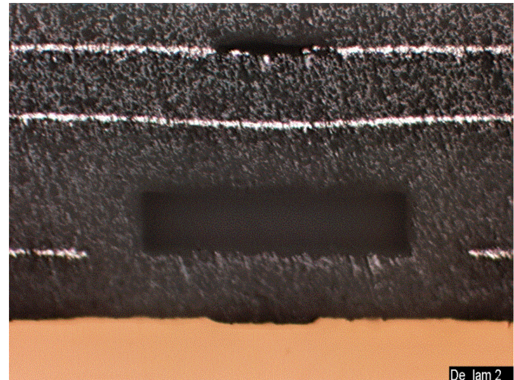

Figure 9. Delamination has occurred at a layer interface containing metallization

Figure 10. The amount, or possibility, of delamination occurring is dependent on location of air cavity relative to other package structures.

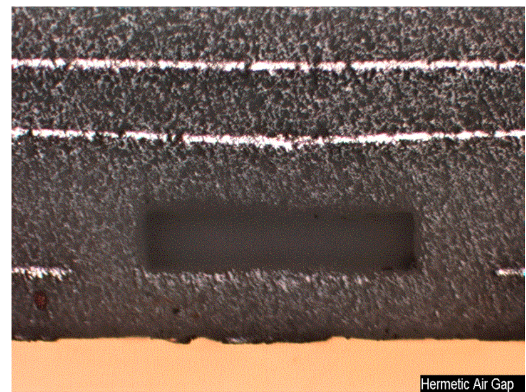

Figure 11. With careful multilayer processes of the air cavity, delamination can be avoided.

Conclusions

The TDR method locates precisely the RF signal path discontinuities that act as performance bottlenecks for broadband package designs. For the leaded package discussed in this paper, the discontinuity between the PCB and multilayer

ceramic package is found to be significantly capacitive. The introduction of air-cavities compensates for the capacitive discontinuity by allowing the effective dielectric constant of the ceramic package to be locally managed and thus significantly reducing the capacitance of the package/lead interconnect. This reduction of capacitance in effect allows the characteristic impedance to be controlled near 50 ohms along the entire signal path in the package. This impedance control greatly improves the broad band electrical performance as demonstrated by computer simulation. As a note, the proposed compensation from the air cavity can be parameterized for semi-custom designs for future packages.

Finally, with careful multilayer processes, the mechanical integrity of the package can be maintained to avoid delamination due to the introduction of sealed air cavities in ceramic packages.

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