Designing Pin Grid Array Ceramic Packages For High Performance in High Density I/O Application

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Abstract:

This work describes the development of a pin-grid array ceramic package (PGA) designed to meet high performance requirements for the Mars Laser Communication Demonstration System (MLCD) undertaken by MIT/LL. As compared to other package types, the PGA package type is not usually, nor has it been historically, considered for very high frequency applications. However, because of legacy system form factor and reliability requirements, a PGA with extended electrical performance is desired. Compounding the challenge of a constrained package form factor is the requirement for increased number and density of high-speed signals. To achieve high-performance from a PGA package, controlled impedance concepts and practices are implemented along the entire signal path. Best performance practices are demonstrated to yield a PGA with performance up to 6 GHz bandwidth in a low-pin density application and up to 3 GHz bandwidth in a high-pin density application.

Introduction

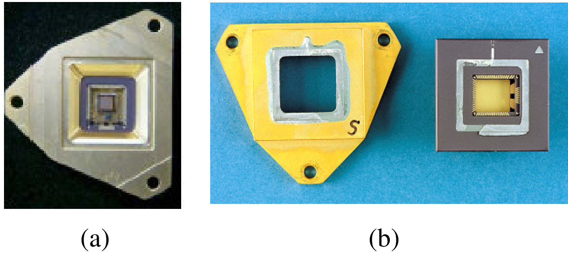
In support of the Mars Laser Communications Demonstration (MLCD) program, Lincoln Laboratory worked on the development of a free-space laser communications system suitable for high rate deep space communications [1]. To demonstrate high-rate communication from Mars, the Link Development and Evaluation System (LDES) would make use of photon-counting Geiger-mode Avalanche Photo Diode (APD) detectors. The anticipation by the National Aeronautics Space Administration is that the demand for long-haul communications between the Earth and deep space locations will require data rates between 1 to 100 Mbits/second [2]. In order to achieve these rates, advances in several technologies are required. In particular, the new signal specifications require the ceramic package for the APD to meet 1Gb/s data rates within legacy package volume constraints. Thusly, RF performance through the package transition has been identified as a major system risk item.

It is demonstrated by full-wave simulation that relatively broadband RF signal performance can be met by a PGA ceramic package incorporating controlled 50-Ohm impedance along each major interconnect of the signal path. To achieve broadband performance, the entire signal path, including the package/interposer transition and the transition between the PGA and printed circuit board (PCB) must be carefully considered. The wire bond details and the number of ground pins between the PCB and PGA become critical limiting factors in the bandwidth of the package. By proper selection of the signal, power, and ground pin number and relative locations, a high signal count package is developed to meet the signal requirements at the PGA/PCB transition. A key feature of the package internal interconnects is the development of high-speed coaxial via structures for controlled impedance paths from the package signal layer to the PGA/PCB transition. These coaxial via structures are shown to provide good signal integrity and good isolation in the band of interest.

Pin-Grid Array Package Design

The basic APD legacy PGA package and mount considered for redesign is shown in Figure 1a. The APD resides on a ceramic interposer, which is placed inside the ceramic package above a thermo-electric cooler. The mount is FeNiCo and the ceramic package is alumina (ε_r=10). Figure 1b shows the APD mount and the APD Kyocera ceramic package, unassembled at the copper-silver braze-joint between the FeNiCo APD mount and the alumina package substrate. The package outline is approximately an inch square. To incorporate new designs, the cavity was increased in size; however the square outline of the ceramic package was constrained to remain fixed. This constraint is necessary to ensure that fixtures inside the system, which

connect to the package/mount, do not have to be re-engineered. This provides a great reduction in non-recurring engineering and allows a drop-in solution for the package.



(a) (b)

Fig. 1: The APD, Kyocera package and mount a) Assembled view, b) mount and ceramic package

Because of the increasing speed and signal density requirements, the APD detector packages have changed over the last several years from a 69-pin design to the current 160-pin design as depicted in Figure 2. These new requirements necessitate the need for impedance control concepts to be employed for each high-speed interconnect and transition of the signal paths in order to preserve and improve signal integrity.

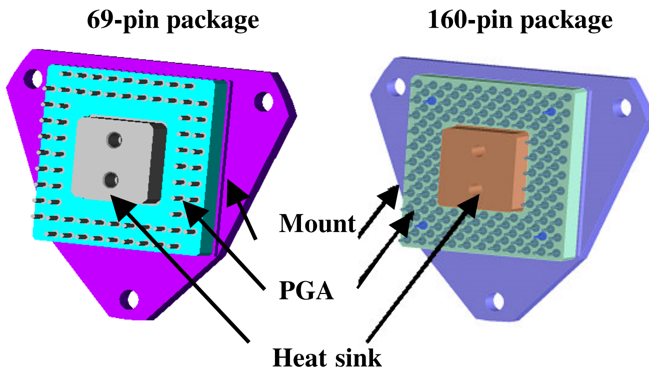


Fig. 2: The 69-pin and 160-pin PGA

In Figure 3, (a cross-section of a conceptual view of the interposer, ceramic package, and printed circuit board (PCB)) the signal path from the interposer to the PCB is traced. The interposer material is aluminum nitride, AlN, 15-mils thick with a dielectric constant of 8.6. The type and location of each critical transition along the interconnect path can be identified by inspection. The transition from the interposer to the ceramic package is a set of wire bonds. The wire bonds connect pads on the interposer to a set of grounded coplanar waveguide (CPWG) traces on the package. The CPWG traces transition to striplines, which in turn connect to an RF via. The RF via will eventually be connected to the pin of the PGA. To obtain broadband performance from the PGA, controlled impedance methods and best engineering practices need to be employed.

Interposer/package Transition

Using the principle of designing packages by following the signal from the device to the board, we see that the first major transition that can limit electrical broadband performance is the wire bond transition. The best performing wire bond transition between the interposer and the package is achieved by keeping wire bonds as short as possible and placing signal pads on the interposer between ground pads, i.e. a ground-signal-ground configuration as shown in Figure 4.

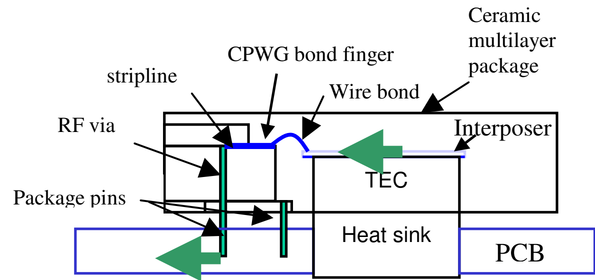


Fig. 3: Cross-section of interposer, ceramic package, PCB interconnect concept.

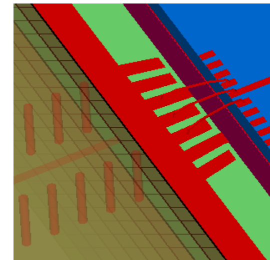


Fig. 4: Wire bond transition from interposer to package substrate

The device, not shown in the Figure, is located on the interposer. Microstrip traces on the interposer connect the device to the interposer pads, which in turn connect to the package with gold wire bonds. The wire bonds are 1-mil in diameter and connect to the bond fingers on the package across a 40-mil gap between the interposer and the package. The bond pads, which form a short coplanar waveguide segment on the package, are 20-mils above a ground plane. The appropriate width of the bond finger and the CPWG segment is kept at 10-mils. The CPWG transitions to a 50-Ohm, 6-mils wide stripline interconnect.

The performance of this wire bond transition is shown in Figure 5. The return loss, S11, and the insertion loss, S21, has good to fair performance across the band defined from 0 to 15 GHz, and good performance across the specific band of interest, 0 to 5 GHz. Although,

optimization techniques can be employed for this wire bond transition, the eventual number of desired high-speed signals limits the required area compensating impedance matching structures.

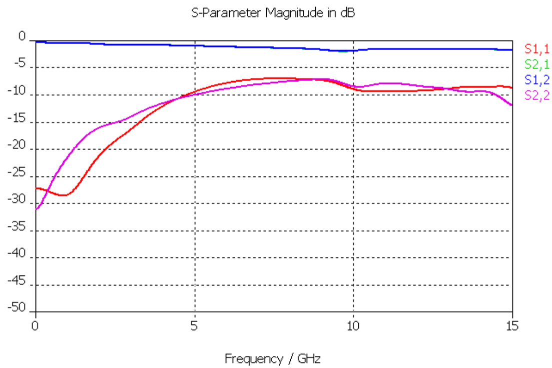


Fig. 5: The S-parameters for the wire bond transition from interposer to CPWG on ceramic package.

Impedance Control with the Coaxial Via Structure

The next major segment in the interconnect path from the device to the PCB is the stripline to package pin connection. The underlying principle for designing this transition of the high-speed interconnects is to limit the number of intervening transitions between the stripline and the pins of the package. Ideally, a straight down interconnect will provide the optimum choice. The approach taken in this paper is to use the coaxial via structures [3] as illustrated in Figure 6. The signal vias connecting the stripline to the pin is surrounded by a few strategically placed grounding vias. In this work we have used a 2D quasi-static tool [4] to investigate and to design the precise number and location of ground vias needed to maintain 50-Ohm characteristic impedance along the coaxial via.

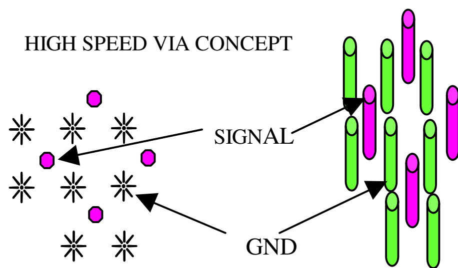


Fig. 6: High-speed coaxial via structure concept.

Figure 7 shows a number of high-speed coaxial via structures considered for tradeoff analysis. The tradeoff is between the required area for each configuration and its corresponding electrical performance, which in this case is the provided isolation between coaxial via structures. The necessary area for the coaxial via structure is defined as the clearance opening that would be required in any intervening ground plane between the stripline and the pin to allow clearance for the signal via while simultaneously maintaining connection to the ground via.

Figure 7a illustrates a coaxial via structure using only 2 vias, one for the signal and one for the ground path. The required real estate is defined as the needed clearance hole of radius 15.35-mils to meet the definitions described previously. This radius, which also defines via pitch is not manufacturable in the selected process, but will be regarded for comparison purposes only. The coaxial via structure in Figure 7b and 7c are variations of a coaxial via structure using 3 vias, 1 via for the signal, and two vias for the ground path. In Figure 7b, ground vias are placed in line and on either side of the signal via. In 7c, the ground vias are located in a triangular arrangement at a minimum of 20-mils with a radius of 21-mils. Figure 7d and 7e are variations of a coaxial via structure using 4 vias, 1 via for the signal and 3 vias for the ground path. In 7d, symmetry in location of the ground vias is preserved, whereas in 7e, the via located closest to the signal via is kept at a constant pitch of 20-mils while the location of the two other ground vias is determined by the 50 Ohm target characteristic impedance. The corresponding clearance hole for this coaxial via structure is determined to be an ellipse. In Figure 7f, 4 ground vias are symmetrically placed around a signal via for a coaxial via structure using 5 vias. In figure 7g, a coaxial via structure using 13 vias is used to closely approximate an ideal coax having a solid outer ground shroud.

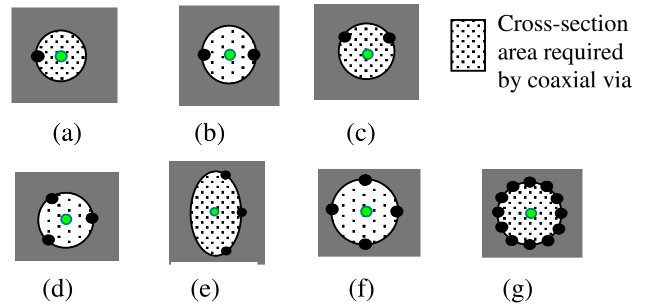


Fig. 7: A number of coaxial via structures considered: a) 2 vias b) 3 vias in line, c) 3 vias in triangular configuration, d) 4 vias, e) 4 vias, ellipse configuration, f) 5 vias, g) 13 vias

It is obvious that there are innumerable combinations of via configurations enabling a 50-Ohm impedance to be realized by the coaxial via structure. Nevertheless there is a minimum cross-section area required for each coaxial via structure determined by both the number of ground vias and the configuration of these ground vias relative to the location of the signal via. In Figure 8, we plot the required cross-sectional area for the coaxial via structures of Figure 7 as a function of the total number of vias in the coaxial via structure. The corresponding clearance hole radius for the circular coaxial

via structures is also plotted. Two log-trend lines are placed to trace the increase in required real estate and clearance hole radius as the number of vias increases from a minimum of two vias to a maximum determined by the manufacturing process. As is well known from transmission line theory, the maximum cross-sectional area for the coaxial via structure is determined by the diameter of the signal via (7 - mils for selected process) and the case where the ground is a solid shroud. If enough ground vias are used to approximate the solid coax shroud, and kept within the design rule limits, the maximum cross-sectional area of the coaxial via structure is 7542 sq mils (a clearance opening having a radius of about 49-mils).

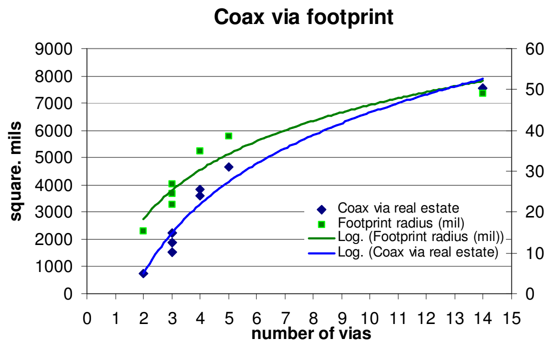


Fig. 8: The cross-section area and clearance hole radius for various via coaxial via structures.

Given the numerous coaxial via structures possible for establishing a 50-Ohm impedance transmission line from the top signal layer of the package to the package pins, a tradeoff is required to select the optimum coaxial via structure. The optimum structure is selected by trading off between the required cross-sectional area and the cross-talk isolation provided by each coaxial via structure in the frequency of operation.

Cross-coupling Simulation and Analysis for Coaxial Via Structure

For a PGA package that has 160 pins, a simplified model and analysis prevails in the selection of the appropriate coaxial via structure. Figure 9 shows the stack-up of the 4 coaxial via structures used for comparison in cross-coupling performance. The test package is 250 mils thick and has a microstrip line on the top layer connected to a stripline in the last layer of the coaxial via structures shown. Port 1 and 3 (P1, P3) define ports of microstrip 10-mils above a ground plane. Port 2 and port 4 define ports of stripline in a 28-mil thick section of the multilayer ceramic package. Figure 9a shows a top and side view of two closely spaced parallel coaxial via structures comprised of 2 vias in each coaxial via structure. Figure 9b shows a top and side view of two closely spaced parallel coaxial via structures comprised of 3 vias in each coaxial via structure. Figure 9c shows a top and side view of two closely spaced parallel coaxial via structures comprised of 4 vias in each coaxial via structure, and, finally, Figure 9d shows a top and side view of two closely spaced parallel coaxial via structures comprised of 5 vias in each coaxial via structure.

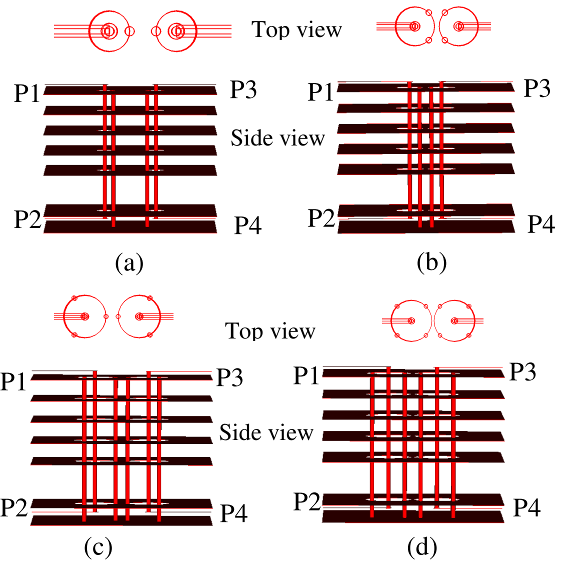


Fig. 9: Four coaxial via structures considered for isolation study: a) 2 vias, b) 3 vias, c) 4 vias, d) 5 vias.

Figure 10 shows the return loss for each configuration in a tightest possible manufacturable location. The two coaxial via structures in Figure 9a have a signal pitch of 50.7-mils. The three coaxial via structures in Figure 9b have a signal via pitch of 54.6-mils. The four coaxial via structures of Figure 9c have a signal via pitch of 90-mils and the five coaxial via structures in Figure 9d have a signal via pitch of 81-mils. These pitches are defined by the minimum via pitch of 20-mils. For the coaxial via structure using 5 vias (Fig. 9d), the smallest printable conductor width between ground openings (4-mils) determines the signal pitch. As shown from inspection of Figure 10, the return loss for the various coaxial via structures improves as the number of ground pins increases.

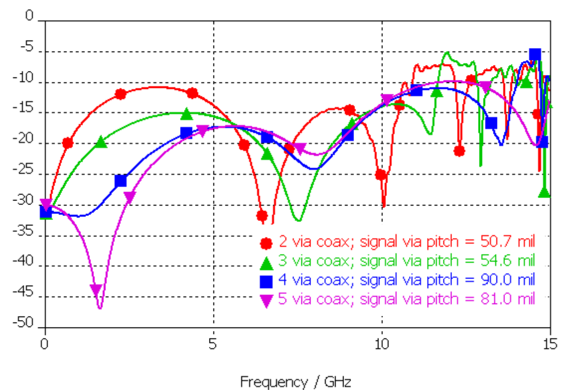


Fig 10: Return loss of coaxial via structures using 2, 3, 4 and 5 vias. Signal pitch is determined by densest manufacturing

Figure 11 shows the insertion loss for the coaxial via configurations illustrated in Figure 9 with the tightest manufacturable signal pitches. Again it is shown that the bandwidth improves as the number of ground vias in the coaxial configuration increases. For the case of 2 vias, the

bandwidth is roughly from 1 to 10 GHz. This is improved to nearly 15 GHz by moving to a 5 via coaxial via structure.

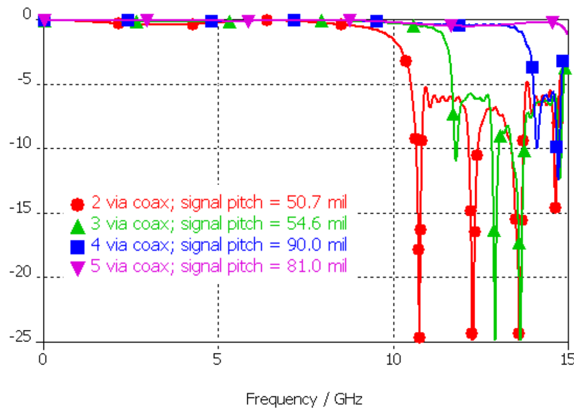


Fig. 11: Insertion loss for 2-, 3-, 4-, and 5 via coaxial via structures. Signal pitch is determined by densest manufacturing capability.

Figure 12 shows the coupling from port 1 to port 3, from microstrip port to microstrip port. As expected, the isolation is improved by increasing the number of ground vias. All configurations exhibit -30 dB of isolation below 6 GHz.

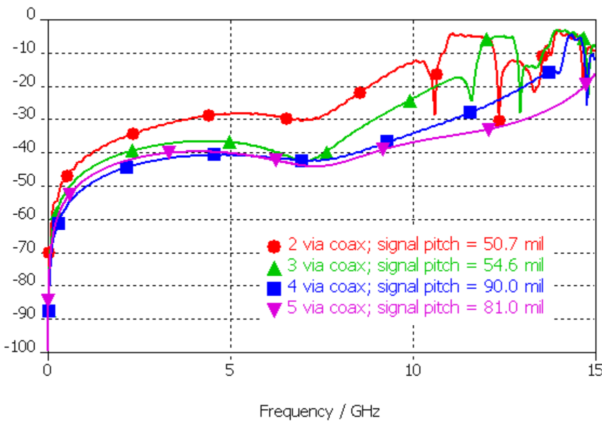


Fig. 12: Cross-coupling from port 1 to port 3 for 2-, 3-, 4-, and 5- via coax configurations. Signal pitch is determined by densest manufacturing capability

Figure 13 shows the cross coupling from port 1 to port 4, the coupling from the microstrip port to the stripline port of the adjacent coaxial via structure. As can be seen, the isolation provided by the 2 via coax is poor starting at about 2.5 GHz degrading as the frequency increases. Above 10 GHz, there is no isolation provided at all. Again, as expected the addition of more ground vias improves the isolation. The 3 via coax provides sufficient isolation up to 5 GHz.

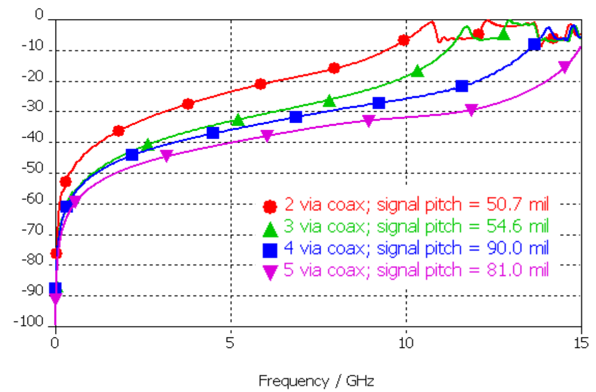


Fig. 13: Cross-coupling from port 1 to port 4 for 2-, 3-, 4, and 5-via coaxial via structures. Signal pitch is determined by densest manufacturing capability

Grounding the Coaxial Via Structure

A frequent design question with regards to the amount of ground required to increase isolation is addressed in this next brief section. As was discussed previously, the coaxial via structure was defined by the required clearance in intervening layers. Each ground via in the coaxial via structure was connected to the intervening ground planes. This is common practice, as is the common practice of printing ground rings connecting the ground vias in the layers that are signal or blank. The following simulations will demonstrate that this grounding technique can and will actually limit the broadband performance of the coaxial via structure.

First, let us again consider the coaxial via structure of Figure 9b and remove the intervening ground planes as illustrated in Figure 14. The grounding of the vias for the microstrip and stripline ground planes remains the same; however the coaxial via structure now has fewer grounding points along the signal path.

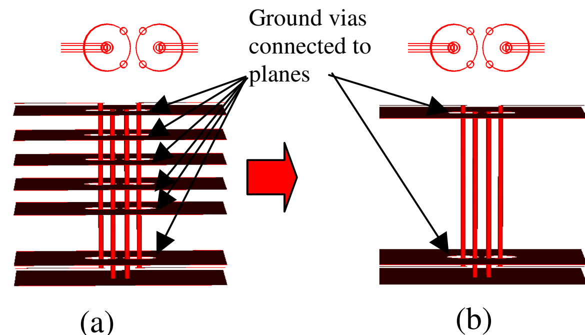


Fig. 14: The coaxial via structure of a) Fig. 9b, and b) intervening ground planes removed.

Figure 15 shows the return loss and insertion loss comparison between the structure in Figure 9b and Figure 14b. It is immediately clear that the bandwidth of the structure without ground via connections to any intervening

planes, other than those defining ground for the microstrip and the stripline, shows marked improvement in the return loss, and more clearly in the insertion loss, which now indicates potential operation to 15 GHz.

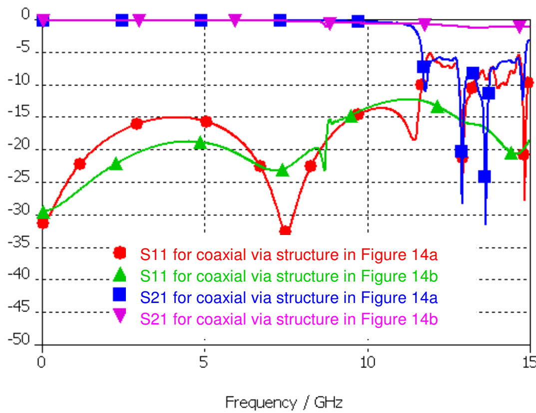


Fig. 15: Return loss and insertion loss comparison between grounding and not grounding the 3-via coaxial via structures with the intervening ground planes.

Examining the simulation results shown in Figure 16 also shows the improvement in reduction of cross coupling. If one defines –30 dB as specified isolation, the grounding of the coaxial via structure at intervening ground planes reduces the bandwidth from about 11 GHz to 6 GHz, a considerable degradation in performance.

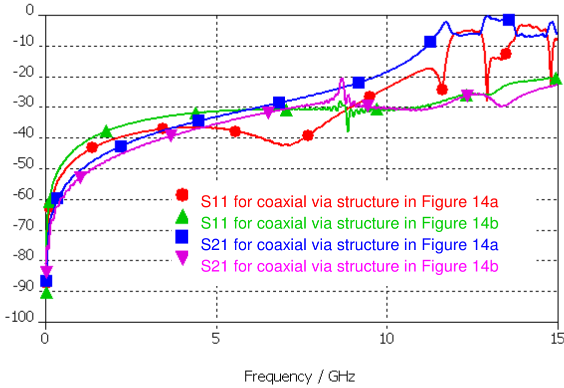


Fig. 16: Cross coupling, S31, S41, for 3-via coaxial via structure connected and not connected to intervening ground planes.

Designing for Low-Pin High-Speed Signals

In the typical PGA design, if we were to implement a high-density approach to the package design we would connect traces from the signal layer to the signal RF vias and connect these RF vias straight down to the pad of the package pin as illustrated in Figure 17. In this figure we have the signal via parallel to two ground vias, but only connected to the PCB ground by 1 pin. Although this is insufficient grounding, it is not unrealistic as many PGA packages utilize the heat sink as the return path for the signal pins, which for low-speed applications is often sufficient. If we select 3 vias in a triangular configuration for the coaxial via structure, as described in the previous discussion, and are free to choose the number of ground pin connections between the ceramic package and the PCB, we can greatly improve the bandwidth of the PGA.

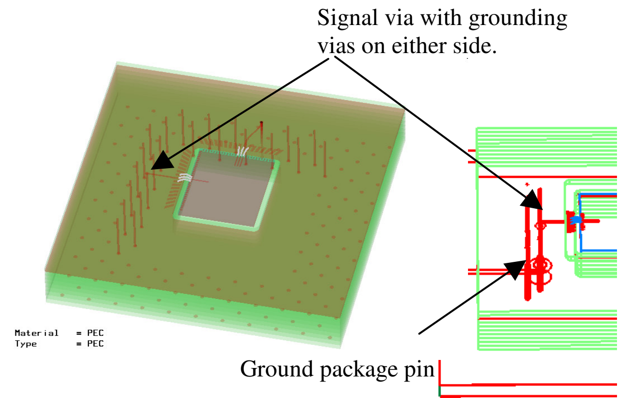


Fig. 17: Illustration of typical via structure for ground and signal in a PGA.

Figure 18 shows a 3-via, triangular configuration for the 50-Ohm coaxial via structure. At the transition between the PCB and the ceramic package, the 4 pins surrounding the signal pin are assigned to ground. This design approach represents a low-pin density high-performance design, since surrounding each high-speed signal path by 4 grounds clearly reduces the number of available pins for high-speed signals.

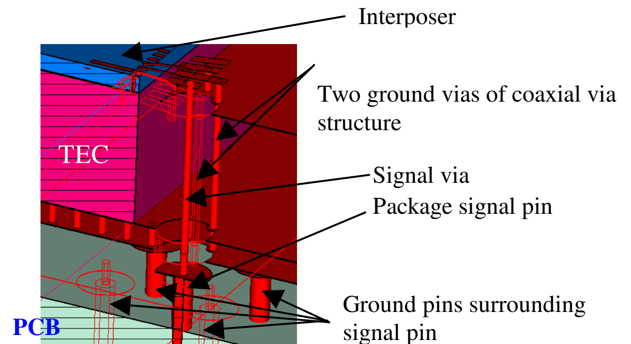


Fig. 18: High-speed coaxial structure and package/PCB transition.

The S-parameters for the structure of Figure 18 are shown in Figure 19. The plots clearly show that a great improvement can be made by establishing controlled impedance from interposer to PCB by the use of coaxial via structure and grounded package pins surrounding the signal pin as it transitions from the package to the transmission line in the PCB. With a –10 dB return loss definition for bandwidth, the high-speed PGA demonstrates a possible 6 GHz bandwidth of operation.

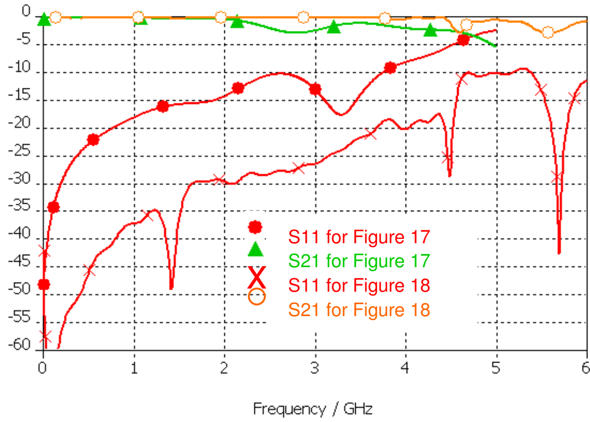


Fig. 19: The S-parameters for a low-speed interconnect of Fig. 17 and high-speed interconnect of Fig. 18

High-Pin Density High-Speed Design Approach

In a real-world application, some degradation in performance must be allowed and accounted for, if we are to increase the number of high-speed signal pins. This tradeoff between the number of high-speed pins and performance is made for the APD ceramic package; the package pin density increased by slightly more than a factor of 2 (from 69 pins to 160 pins), the package must also include pins assigned to various voltages for the packaged device power requirements, and the number of ground pins available for high-speed signals must drop for a desire to have a high-pin density, high-speed signal package.

The complex signal layer routing resulting for a high-pin density, high-speed package is illustrated in Figure 20. This figure shows the high-speed signal layer of the APD package implementing the controlled impedance coaxial via structures.

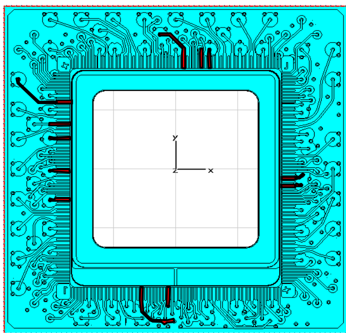


Fig. 20: Signal trace routing implementing stripline transitioning to coaxial-via structure.

The 3-via coaxial via structures between the signal layer and the PGA pins is implemented in as many locations as possible and as close to ideal dimensions as routing, design rules, and the number of needed lower-speed lines allows for the application. All pins near the perimeter of the PGA ceramic package allow close to nominal design parameters for the coaxial via structure to be implemented.

Of course, the high-performance coaxial via structure in the ceramic package will eventually need to transition to the PCB, through the package pin. It would be desirable to assign the pins surrounding each high-speed signal pin to ground, but as discussed previously, this would be impractical in a high-pin density, high-speed package design. To mitigate the limited number of pins available for grounding the package to the PCB, the location of the ground pins relative to the signal pins becomes important. A simple methodology is followed at this stage in assigning the function of the package pins: place as many high-speed pins as close to as many ground pins as possible in a distributed fashion, and place all low-speed signals as dictated by the requirements of the high-speed lines. Figure 21 illustrates the pin assignment for high-speed pins, low-speed pins, two voltages, and ground pins following this methodology. The high-speed pins are placed close to the perimeter of the package, between ground pins, where the coaxial via structure can be implemented. The low-speed signals are placed close to the center of the package where proximity to the package cavity does not allow the coaxial via structure.

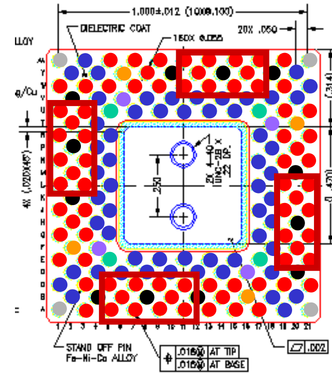


Fig. 21: Pin assignment for high-pin density high-speed PGA package.

After implementing the coaxial via 3-pin design for the high-speed lines in as many locations as routing would allow, we selected typical nets for simulation and measurement correlation. Figure 22 shows the S-parameter performance of a typical high-speed net routed to near the edge of the package. The model and simulation include the transition to a 60 mil Rogers 3003 (ε_r=3.38) multilayer printed circuit board. Good performance, defined by a return loss of -15 dB, is seen out to about 3.5 GHz. Figure 23 shows a typical high-speed net routed to a pin closer to

the cavity and connected to the Rogers PCB. Good performance is shown to about 2 GHz.

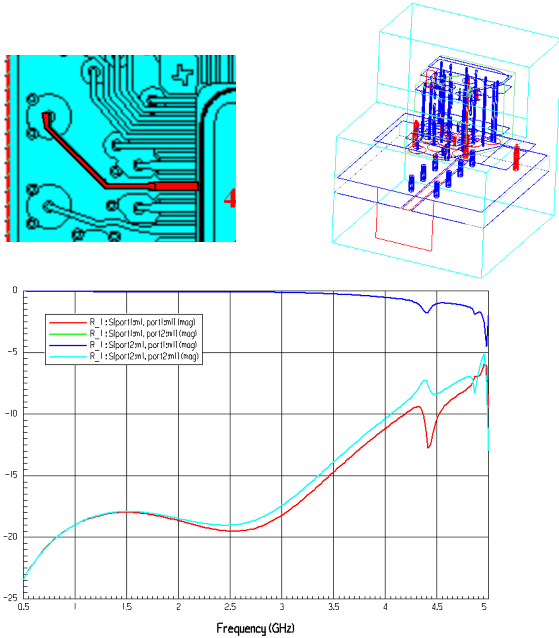


Fig. 22: Insertion and return loss for typical high-speed net routed to package edge in high-density APD package design.

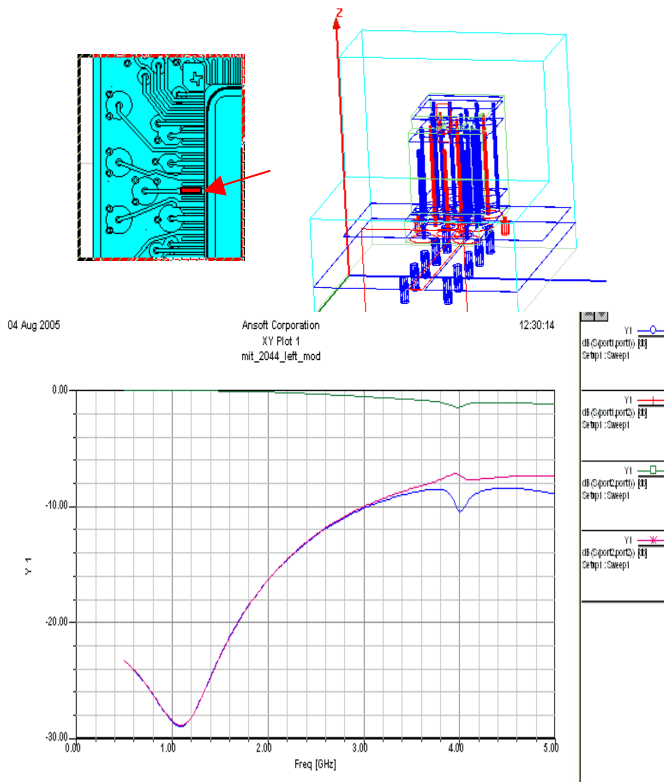


Fig. 23: Insertion and return loss for typical high-speed net routed near to package cavity in high-density APD package design.

Conclusions

A relatively high performance PGA has been designed for the Mars Communication application. With careful attention to controlled impedance techniques it is possible to extend the band of operation of a previous ceramic PGA design beyond frequencies that might previously have been relegated to this type of package. The key coaxial via structure is demonstrated to provide excellent high-speed performance and cross-talk isolation with as little as 1 ground via, and is the only viable method to increase the density of high-speed signal interconnects within the PGA while improving the signal integrity of signal paths within the PGA. To maintain signal integrity, we find that grounding the via at intervening ground planes (or equivalently, placing grounding rings along the via coax) leads to increased cross-talk and should be avoided for high-frequency high-speed interconnects of the coaxial via structures.

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