Transient Thermal Modeling Techniques for WBG Device Packaging

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Outline

- Introduction
- Thermophysical Material Characterization
- Finite Element Global/Submodel Methodology
- Results
- Conclusions

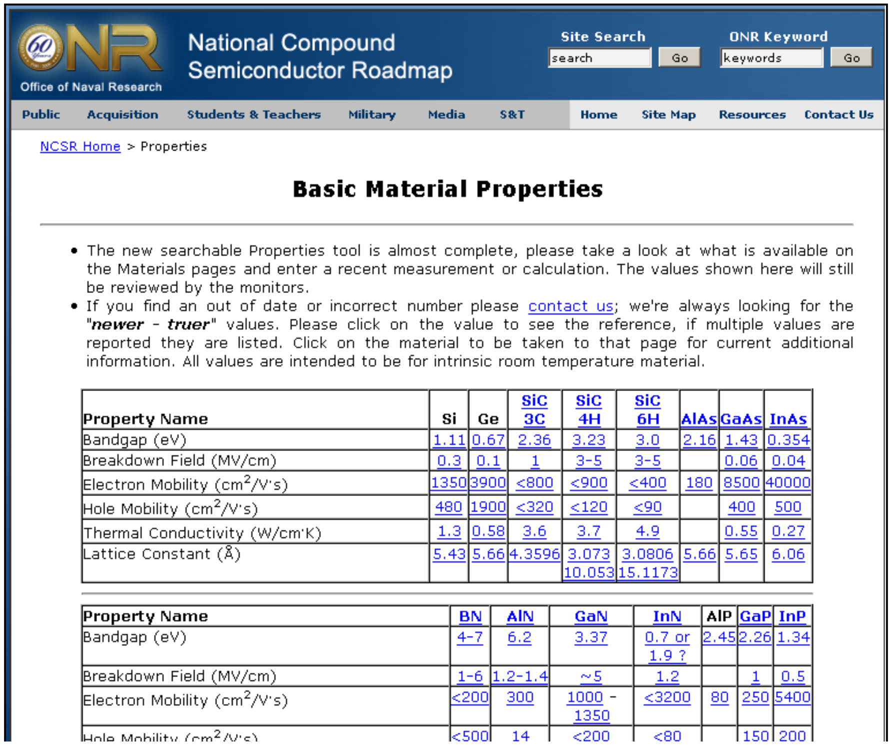
Who is Kyocera America?

Our San Diego facility is a major supplier of metallized ceramic packages for RF and microwave wireless telecom devices. Kyocera America offers a complete line of multilayer ceramic/organic packages for semiconductors in commercial and military markets. We also offer in-house flip-chip and wire-bond packaging services.

Kyocera America, Inc.
Corporate Headquarters
San Diego, CA
www.kyocera.com/kai/

What is a Wide Band Gap (WBG) semiconductor?

- The definition is not very well defined but since a direct comparison of Si seems logical. It is usually taken as 2X the energy band gap of Silicon or approximately 2.0 eV.
- This includes Indium Nitride (InN) all the way up to diamond which is approximately 6.4 eV.
- GaAs is approx 1.4 eV and $Si_{1-x}Ge_x$ is approximately .7~1.1 eV.
- Some good online sources of info/data are:



NCSR Home > Properties

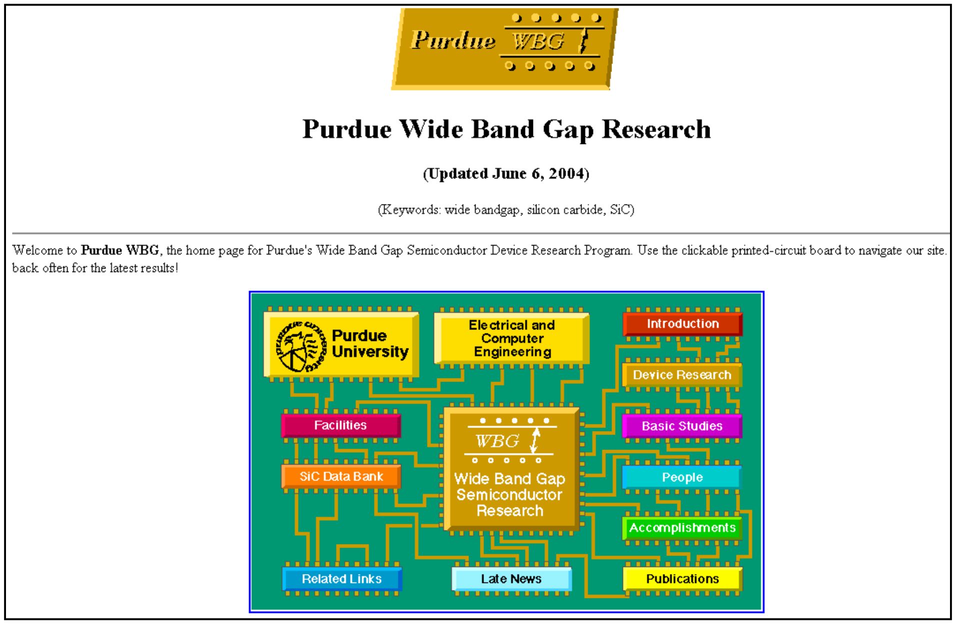
Basic Material Properties

- The new searchable Properties tool is almost complete, please take a look at what is available on the Materials pages and enter a recent measurement or calculation. The values shown here will still be reviewed by the monitors.
- If you find an out of date or incorrect number please contact us; we're always looking for the "***newer - truer***" values. Please click on the value to see the reference, if multiple values are reported they are listed. Click on the material to be taken to that page for current additional information. All values are intended to be for intrinsic room temperature material.

Property Name	Si	Ge	SiC 3C	SiC 4H	SiC 6H	AlAs	GaAs	InAs
Bandgap (eV)	1.11	0.67	2.36	3.23	3.0	2.16	1.43	0.354
Breakdown Field (MV/cm)	0.3	0.1	1	3-5	3-5		0.06	0.04
Electron Mobility (cm^2/V's)	1350	3900	<800	<900	<400	180	8500	40000
Hole Mobility (cm^2/V's)	480	1900	<320	<120	<90		400	500
Thermal Conductivity (W/cm'K)	1.3	0.58	3.6	3.7	4.9		0.55	0.27
Lattice Constant (Å)	5.43	5.66	4.3596	3.073 10.053	3.0806 15.1173	5.66	5.65	6.06

Property Name	BN	AlN	GaN	InN	AlP	GaP	InP
Bandgap (eV)	4-7	6.2	3.37	0.7 or 1.9 ?	2.45	2.26	1.34
Breakdown Field (MV/cm)	1-6	1.2-1.4	~5	1.2		1	0.5
Electron Mobility (cm^2/V's)	<200	300	1000 - 1350	<3200	80	250	5400
Hole Mobility (cm^2/V's)	<500	14	<200	<80		150	200

www.onr.navy.mil/sci_tech/31/312/ncsr/



Purdue Wide Band Gap Research

(Updated June 6, 2004)

(Keywords: wide bandgap, silicon carbide, SiC)

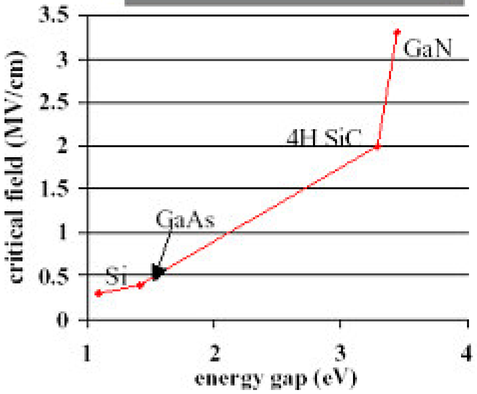
Welcome to **Purdue WBG**, the home page for Purdue's Wide Band Gap Semiconductor Device Research Program. Use the clickable printed-circuit board to navigate our site. Check back often for the latest results!

www.ecn.purdue.edu/WBG/

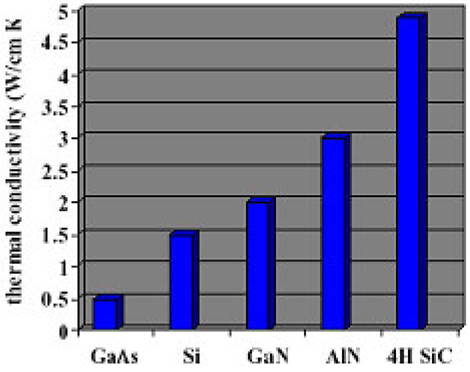
WBG Motivation & Thermal Management

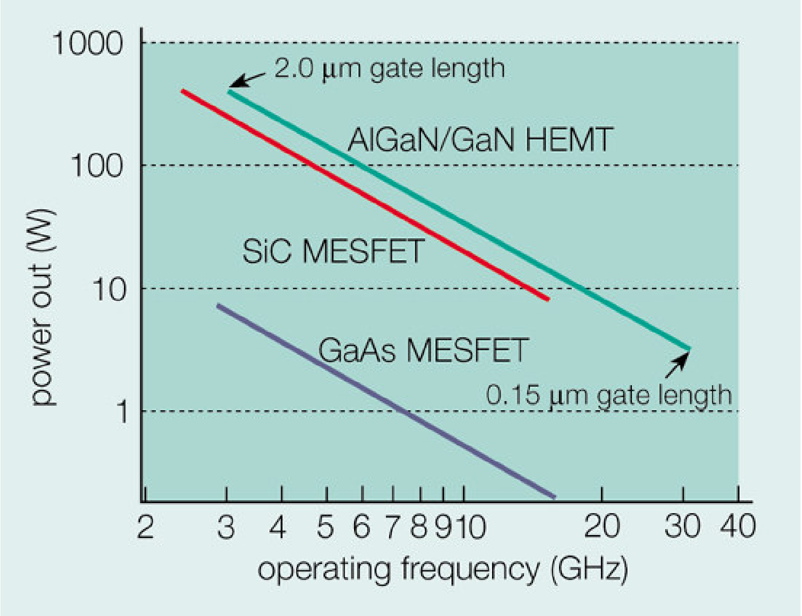
- A large band gap translates to a high breakdown potential which allows the design of power devices that can operate at higher voltages and temperatures (ie higher power density)
- Silicon is frequency limited around ≥ 2.5 GHz. By definition of their excellent electrical transport properties (small dielectric constant and high saturation velocity), WBG semiconductors allow for much higher frequency during operation.
- WBG semiconductor devices would reduce the number of Si based amplifiers in the wireless infrastructure world.
- WBG typically have better thermophysical properties also versus Si.

critical electric field 10x Si and GaAs



SiC thermal conductivity 7x GaAs





Thermophysical Material Characterization

- Recall this is a "transient" analysis discussion thus thermal energy transport is governed by the materials **thermal diffusivity**. Measures the ability of a material to conduct thermal energy relative to its ability to store.

$$\alpha = \frac{k}{c_p \bullet \rho}$$

where:

α = thermal diffusivity (*thermophysical prop*)

k = thermal conductivity (*transport property*)

c_p = specific heat capacity @ constant pressure (*thermodynamic property*)

ρ = density (*thermodynamic property*)

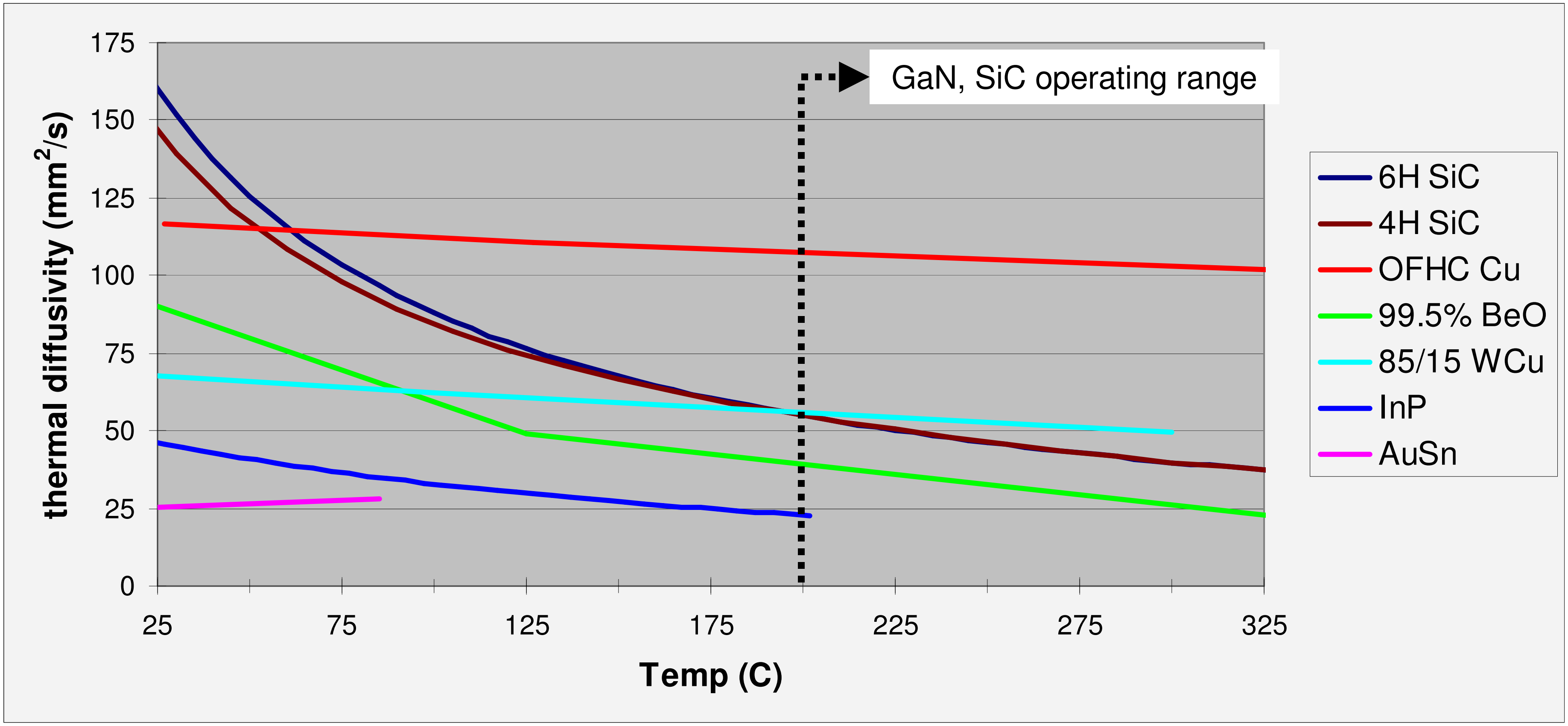
[$c_p \rho$] = volumetric heat capacity

- The performance of electronic systems degrade in proportion to the environment temperature. This temp also determines the service life of the electronic component. An industry rule-of-thumb at or near the design operating temperature states the N_{50} is cut in half for each 10C rise in temp. Excessive high temps can degrade the chemical/structural integrity of various semiconductor devices. Large fluctuations of temp as well as spatial variations of temp in equipment become responsible for most field failures.

The purpose of thermal design is to limit spatial variations and maintain some nominal value.

Thermophysical Material Characterization cont.

BeO, InP, and SiC thermal diffusivity is governed by typical nonconductor phonon transport mechanism (e.g. lattice vibration) and decrease rapidly with inverse of temperature.

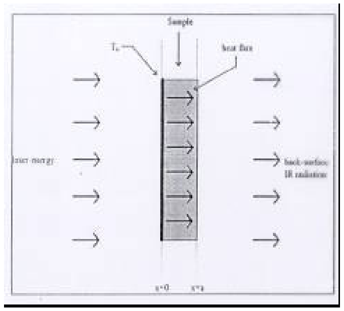


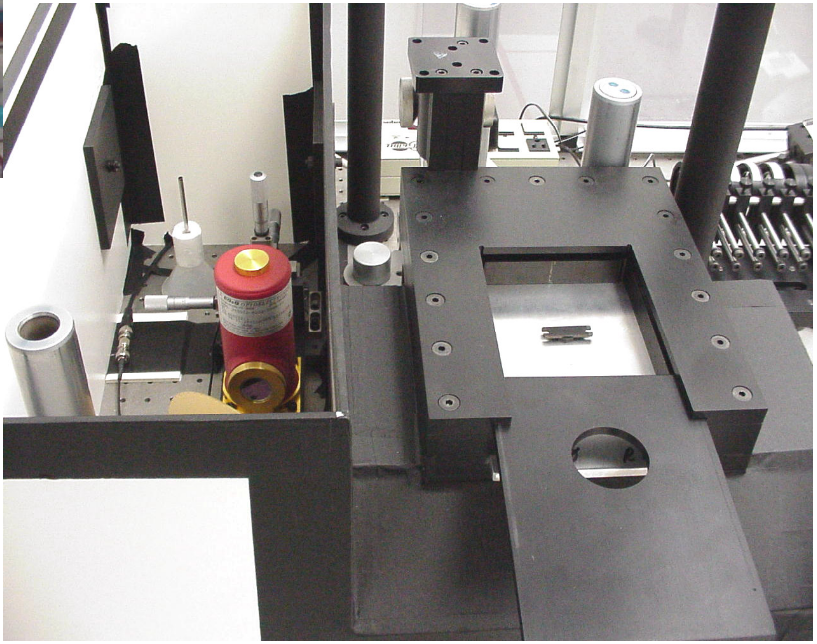
Laser Flash System To Measure Thermal Diffusivity

KAI Proprietary TC System used to validate thermal material properties used in package design (1999).

Description: Custom apparatus measures *thru-plane* thermal conductivity (TC) of a material whose one side has been subjected to a short duration laser pulse. The resultant time vs. temp is monitored by a IR detector. Material TC is resolved by fitting the shape of this temperature rise curve to a 1-D heat flow model.

$$\frac{\partial T}{\partial t} = \frac{\kappa}{\rho C_p} \times \frac{\partial^2 T}{\partial x^2}$$





Closed-Form Solution vs. Simulation

Most thermal pkg design problems are 3D and irregular by nature which don't lend themselves to transient closed-form solutions. The finite element method (FEM) provides us a **robust** numerical technique to solve these specialized cases.

Typical Global Model Results cont.

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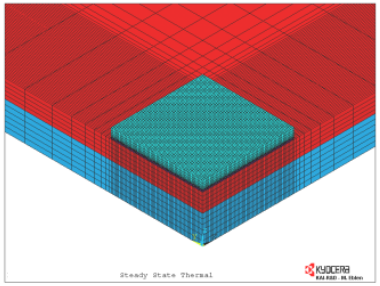
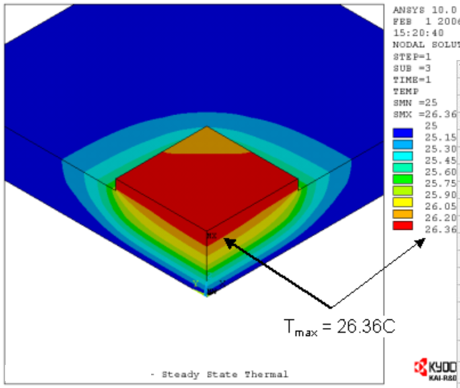


ANSYS™ steady state thermal example

Validate even simple models!



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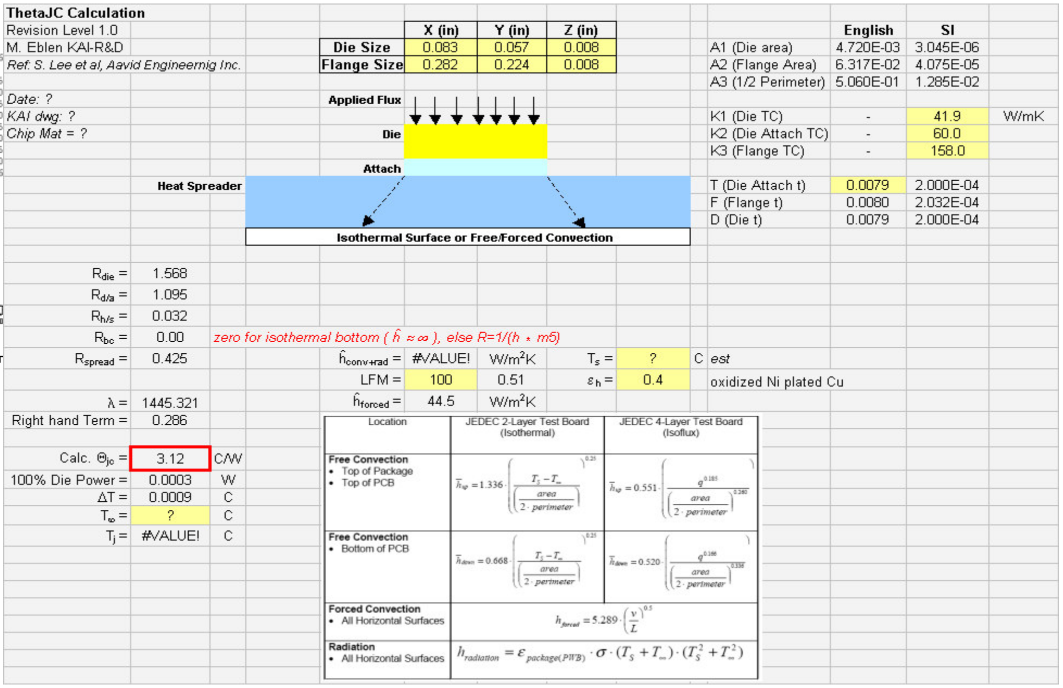
Kyocera America, Inc. Cor



ThetaJC Calculation

Revision Level 1.0

M. Eblen KAI-R&D

Ref: S. Lee et al, Aavid Engineernig Inc.

Date: ?

KAI dwg: ?

Chip Mat = ?

	X (in)	Y (in)	Z (in)
Die Size	0.083	0.057	0.008
Flange Size	0.282	0.224	0.008

	English	SI	
A1 (Die area)	4.720E-03	3.045E-06	
A2 (Flange Area)	6.317E-02	4.075E-05	
A3 (1/2 Perimeter)	5.060E-01	1.285E-02	
K1 (Die TC)	-	41.9	W/mK
K2 (Die Attach TC)	-	60.0	
K3 (Flange TC)	-	158.0	
T (Die Attach t)	0.0079	2.000E-04	
F (Flange t)	0.0080	2.032E-04	
D (Die t)	0.0079	2.000E-04	

R_{die} = 1.568

$R_{d/a}$ = 1.095

$R_{h/s}$ = 0.032

R_{bc} = 0.00 *zero for isothermal bottom ($\hat{h} \approx \infty$), else R=1/(h * m5)*

R_{spread} = 0.425

$\hat{h}_{conv+rad}$ = #VALUE! W/m²K

T_s = ? C *est*

LFM = 100 0.51

ε_h = 0.4 oxidized Ni plated Cu

$\hat{h}_{forced}$ = 44.5 W/m²K

λ = 1445.321

Right hand Term = 0.286

Calc. Θ_{jc} = 3.12 C/W

100% Die Power = 0.0003 W

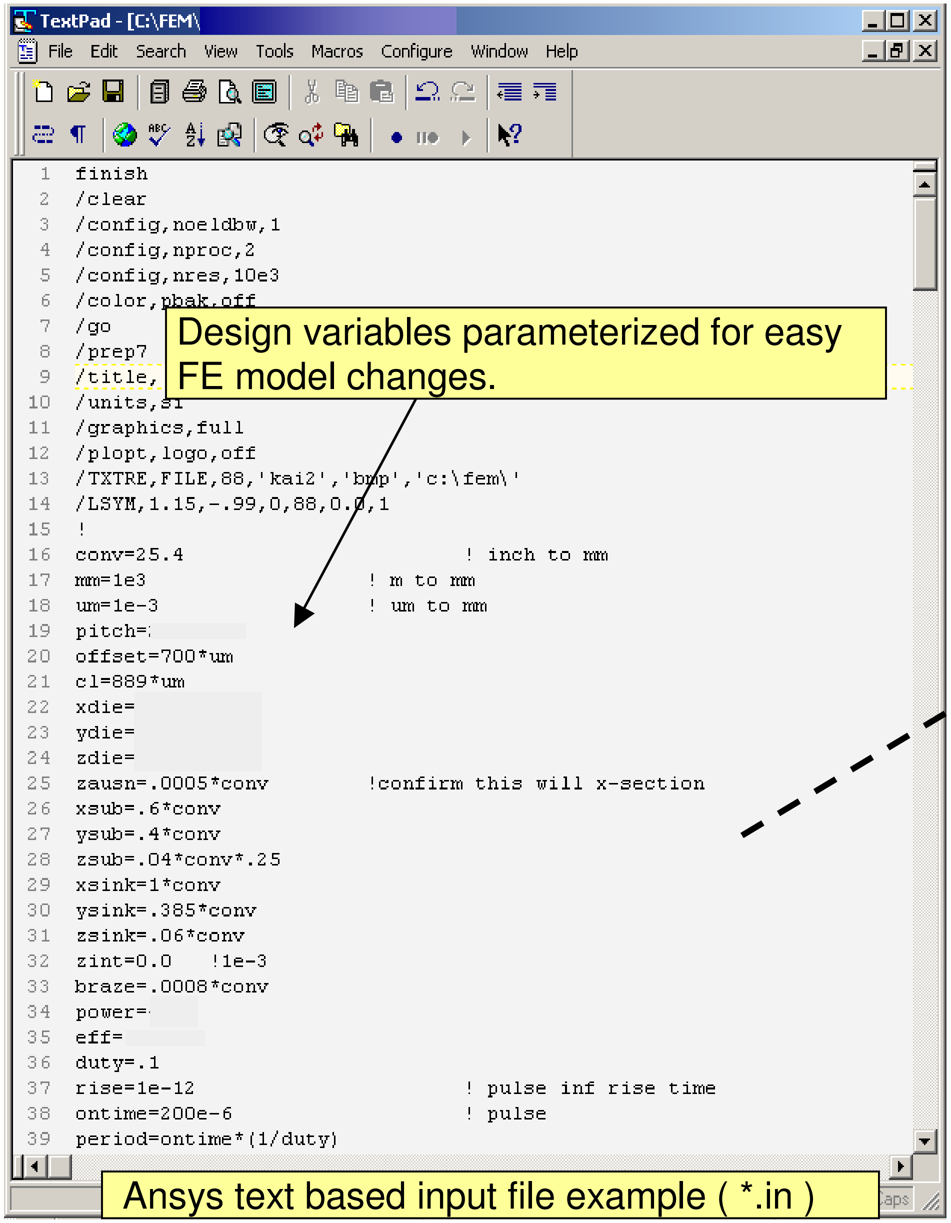
ΔT = 0.0009 C

T_∞ = ? C

T_j = #VALUE! C

Location	JEDEC 2-Layer Test Board (Isothermal)	JEDEC 4-Layer Test Board (Isoflux)
Free Convection • Top of Package • Top of PCB	$\bar{h}_{up} = 1.336 \cdot \left(\frac{T_S - T_\infty}{\left(\frac{area}{2 \cdot perimeter} \right)} \right)^{0.25}$	$\bar{h}_{up} = 0.551 \cdot \left(\frac{q^{0.185}}{\left(\frac{area}{2 \cdot perimeter} \right)^{0.280}} \right)$
Free Convection • Bottom of PCB	$\bar{h}_{down} = 0.668 \cdot \left(\frac{T_S - T_\infty}{\left(\frac{area}{2 \cdot perimeter} \right)} \right)^{0.25}$	$\bar{h}_{down} = 0.520 \cdot \left(\frac{q^{0.166}}{\left(\frac{area}{2 \cdot perimeter} \right)^{0.338}} \right)$
Forced Convection • All Horizontal Surfaces	$h_{forced} = 5.289 \cdot \left(\frac{v}{L} \right)^{0.5}$	
Radiation • All Horizontal Surfaces	$h_{radiation} = \varepsilon_{package(PWB)} \cdot \sigma \cdot (T_S + T_\infty) \cdot (T_S^2 + T_\infty^2)$	

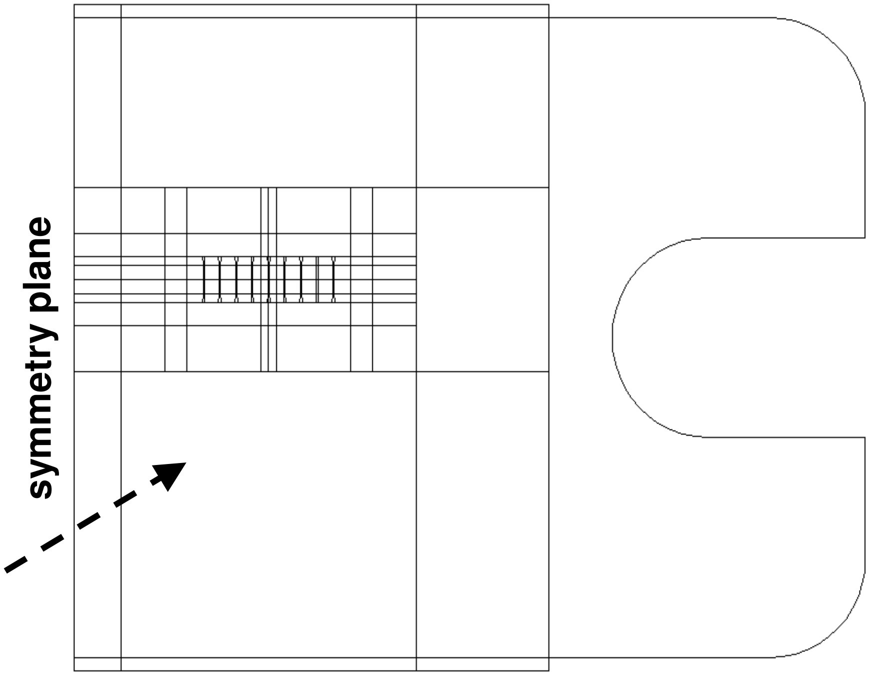
ANSYS™ FE Model File Description Hierarchy



```
finish
/clear
/config,noeldbw,1
/config,nproc,2
/config,nres,10e3
/color,pbak,off
/go
/prep7
/title,
/units,si
/graphics,full
/plopt,logo,off
/TXTRE,FILE,88,'kai2','bmp','c:\fem\'
/LSYM,1.15,-.99,0,88,0.0,1
!
conv=25.4                               ! inch to mm
mm=1e3                          ! m to mm
um=1e-3                         ! um to mm
pitch=[redacted]
offset=700*um
cl=889*um
xdie=[redacted]
ydie=
zdie=
zausn=.0005*conv                !confirm this will x-section
xsub=.6*conv
ysub=.4*conv
zsub=.04*conv*.25
xsink=1*conv
ysink=.385*conv
zsink=.06*conv
zint=0.0     !1e-3
braze=.0008*conv
power=[redacted]
eff=[redacted]
duty=.1
rise=1e-12                              ! pulse inf rise time
ontime=200e-6                           ! pulse
period=ontime*(1/duty)
```

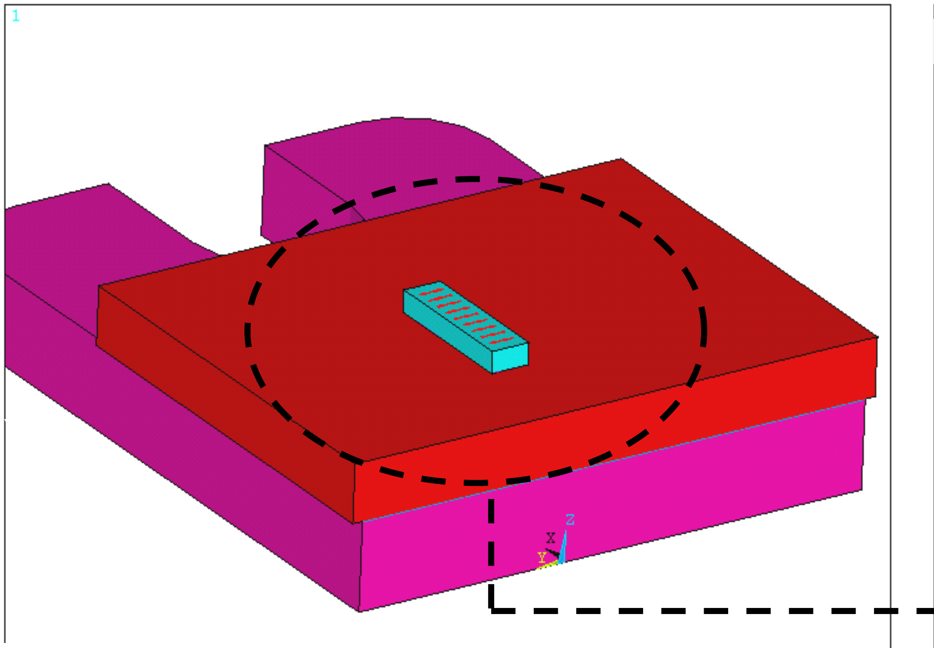
Design variables parameterized for easy FE model changes.

Ansys text based input file example (*.in)

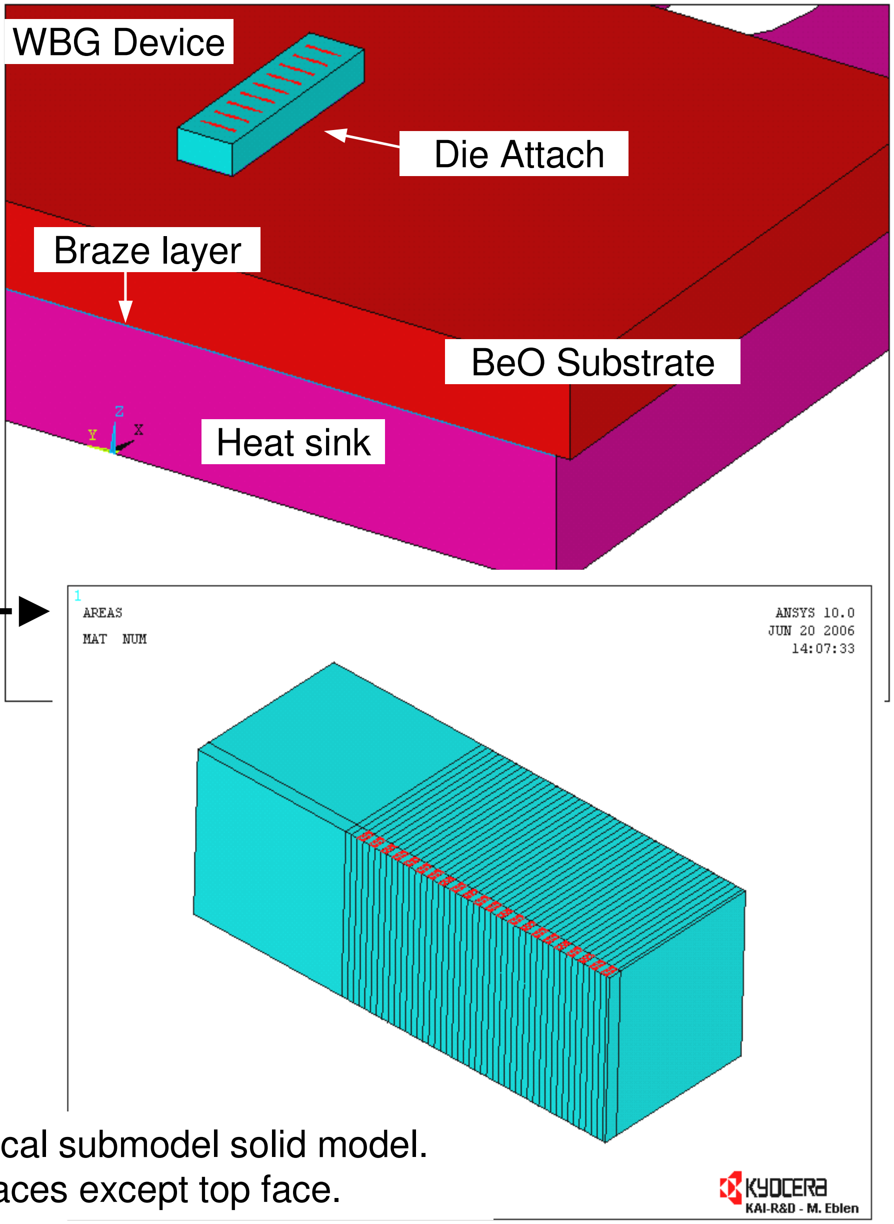


ANSYS input file calls 2D IGES geometry file. Drawing areas are sub-divided for better mesh control.

WBG Example: Bipolar RF Ceramic Package

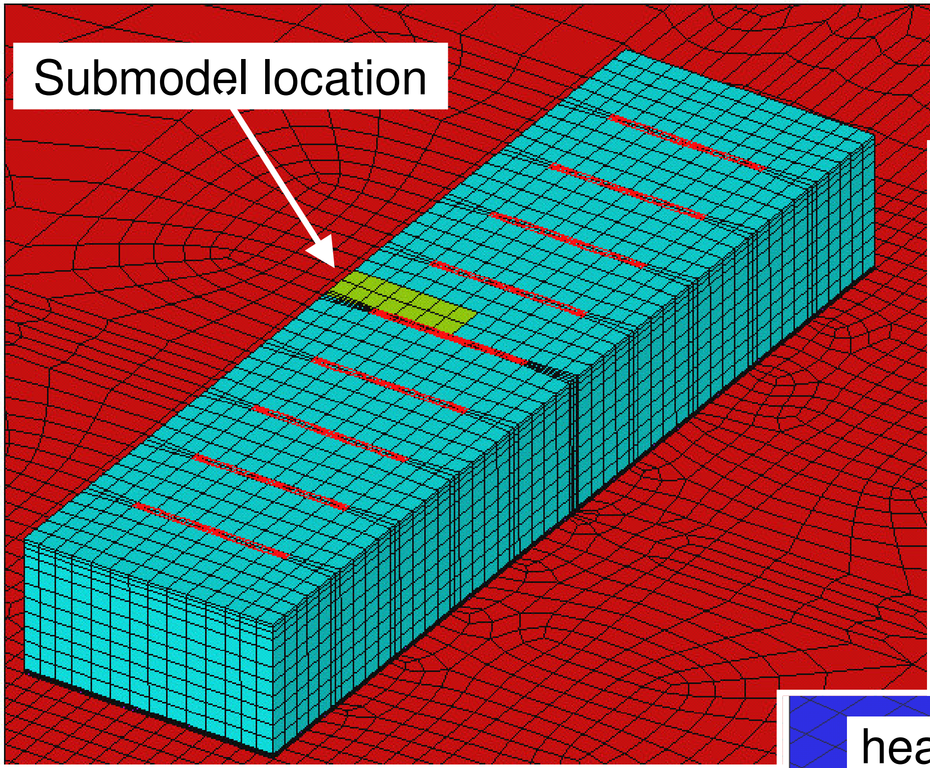


½ symm course mesh global solid model

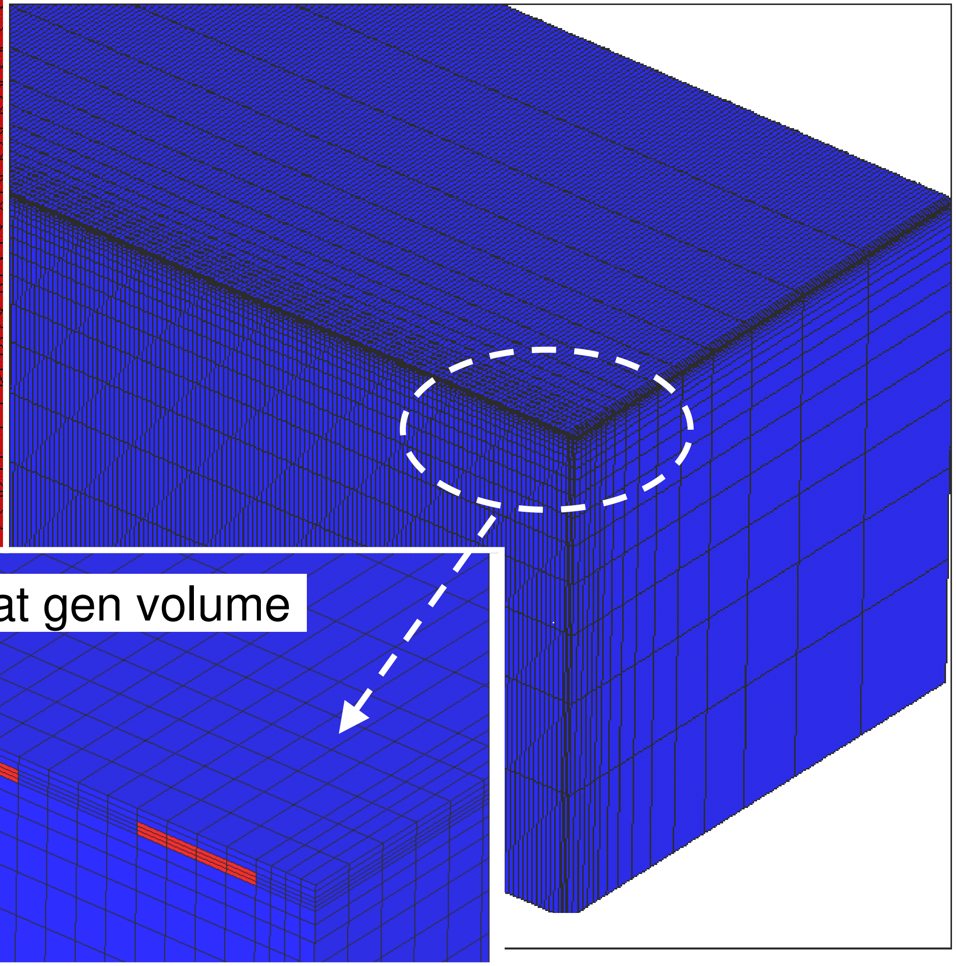


Detailed view of ¼ symmetric typical submodel solid model.
Thermal bc’s specified on all surfaces except top face.

FE Submodel Technique for Increased T(t) Resolution



Course mesh global model with ½ symmetric submodel volume outline shown in **green**.



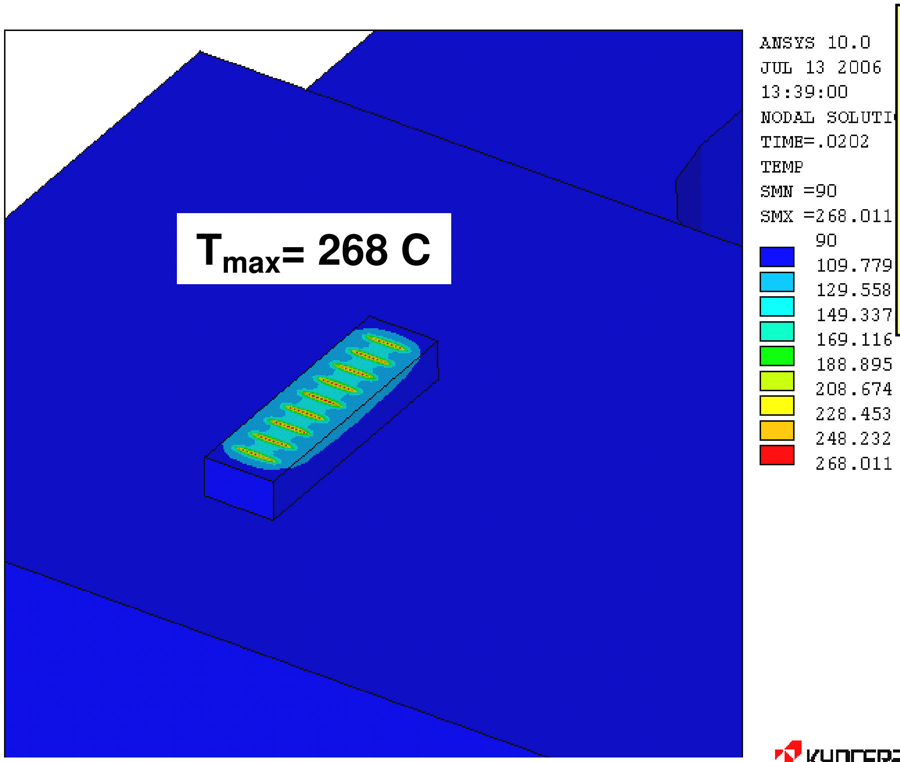
Detailed view of ¼ symmetric submodel. Thermal bc’s specified on all surfaces except top face and symmetric planes.

WBG Bipolar RF Ceramic Package Results

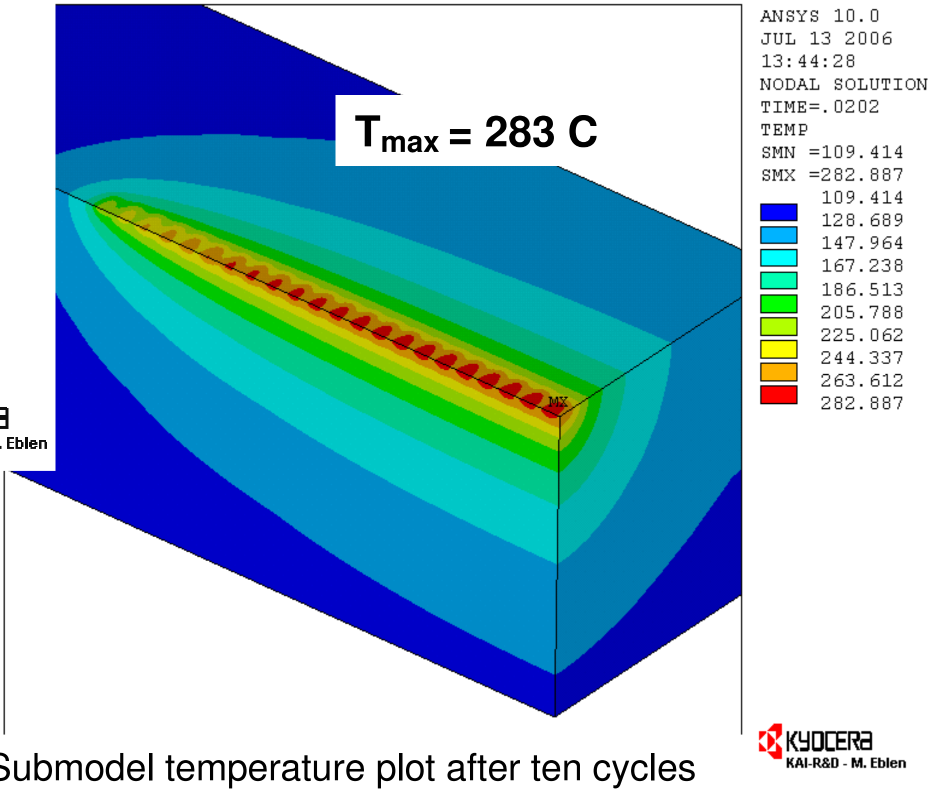
Transient Analysis Conditions:

200us pulse width @ 10% duty cycle

Bottom global model prescribed at 90C for this example, typically an effective convection coefficient is used (W/mm^{2}K).



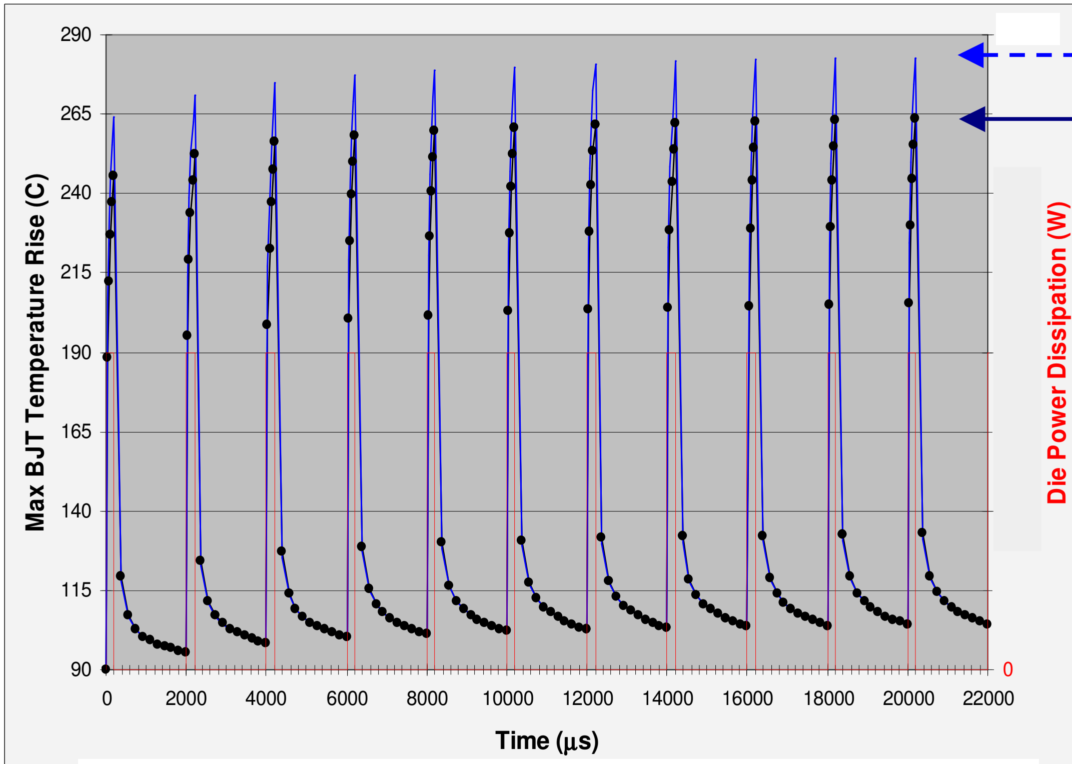
Global model temperature plot after ten cycles with WCu heat sink



Submodel temperature plot after ten cycles

WBG Bipolar RF Ceramic Package Results

Device is not operated in a continuos ″on″ state, a transient analysis must be conducted considering the time varying power pulse [e.g. P(t)].



10% Duty Cycle Transient ΔT History.

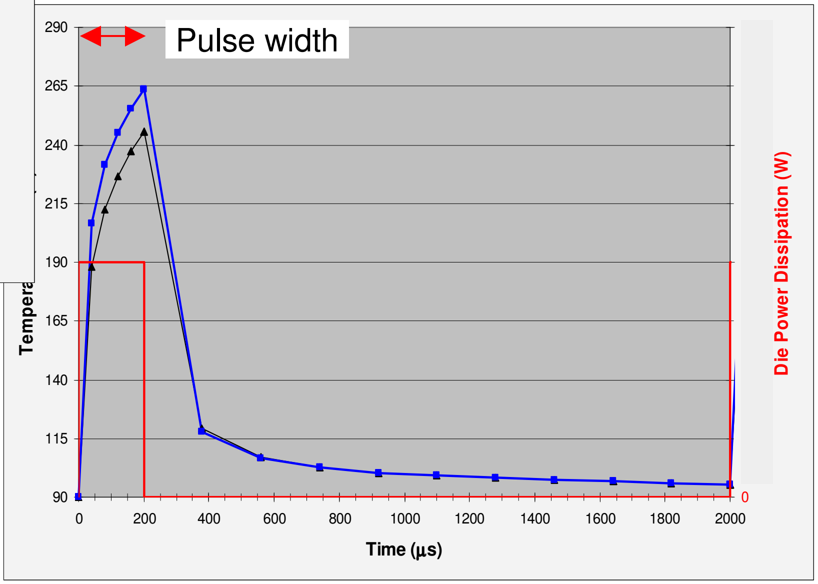
Quasi-steady state sub-model max T_j=283C

15 °C resolution due to submodel technique

Quasi-steady state global max T_j =268C

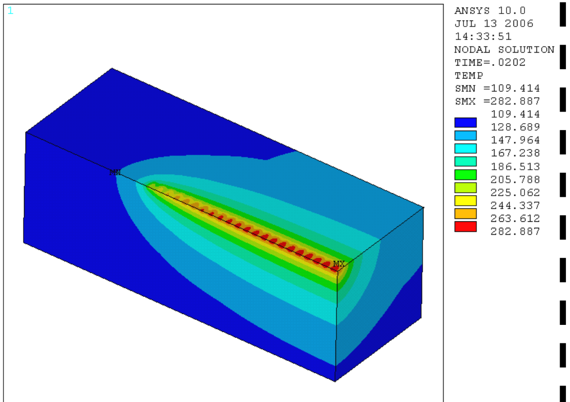
We will define the "on-time" of the cycle to be when the output is high, and the "off-time" when the output is low. Duty-cycle is defined to be:

$$\text{Duty-Cycle} = \frac{\text{On-Time}}{\text{On-Time + Off-Time}}$$



Detailed View of Initial Pulse.

WBG Bipolar RF Ceramic Package Results



Submodel temp plot

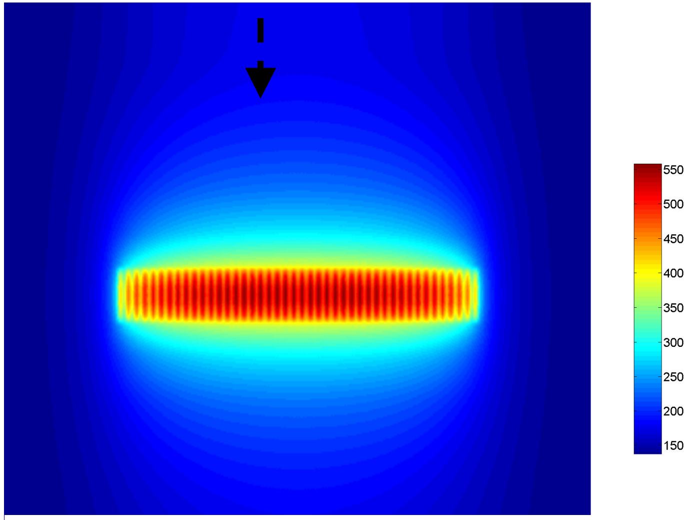
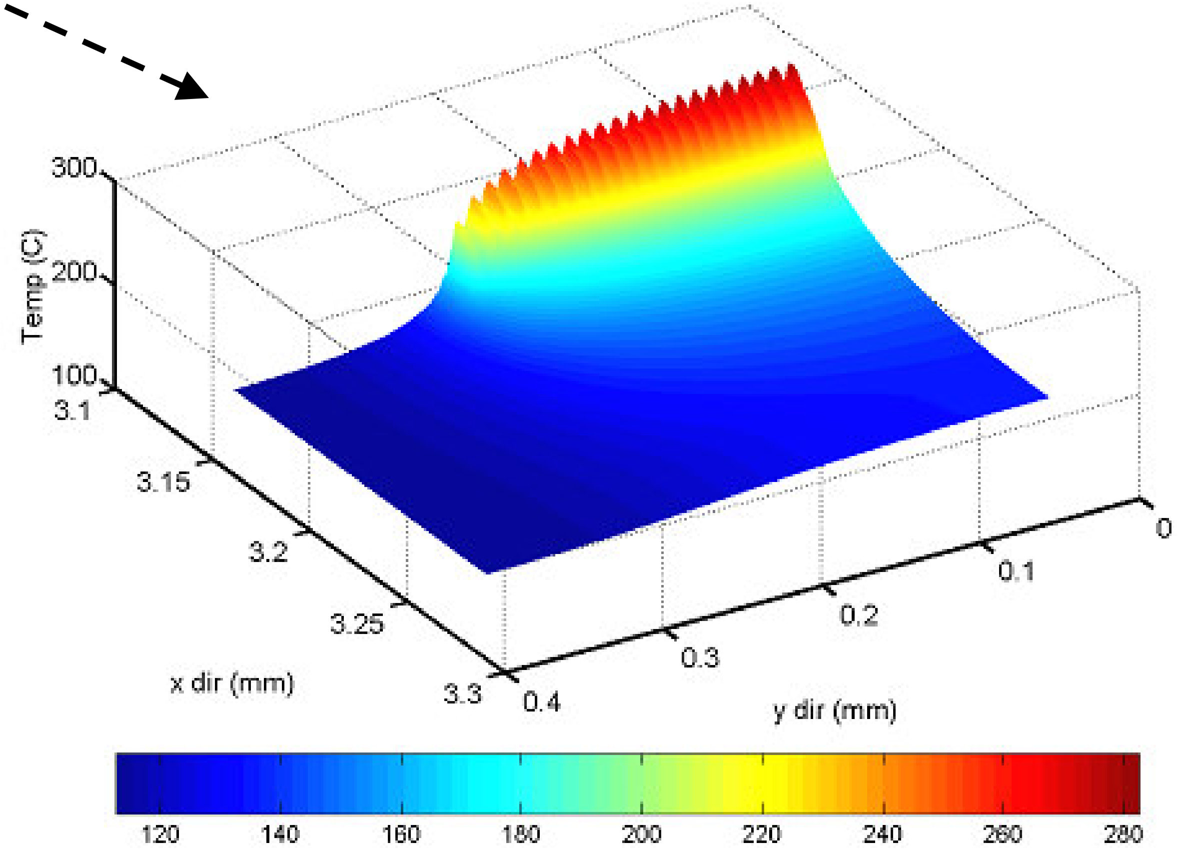


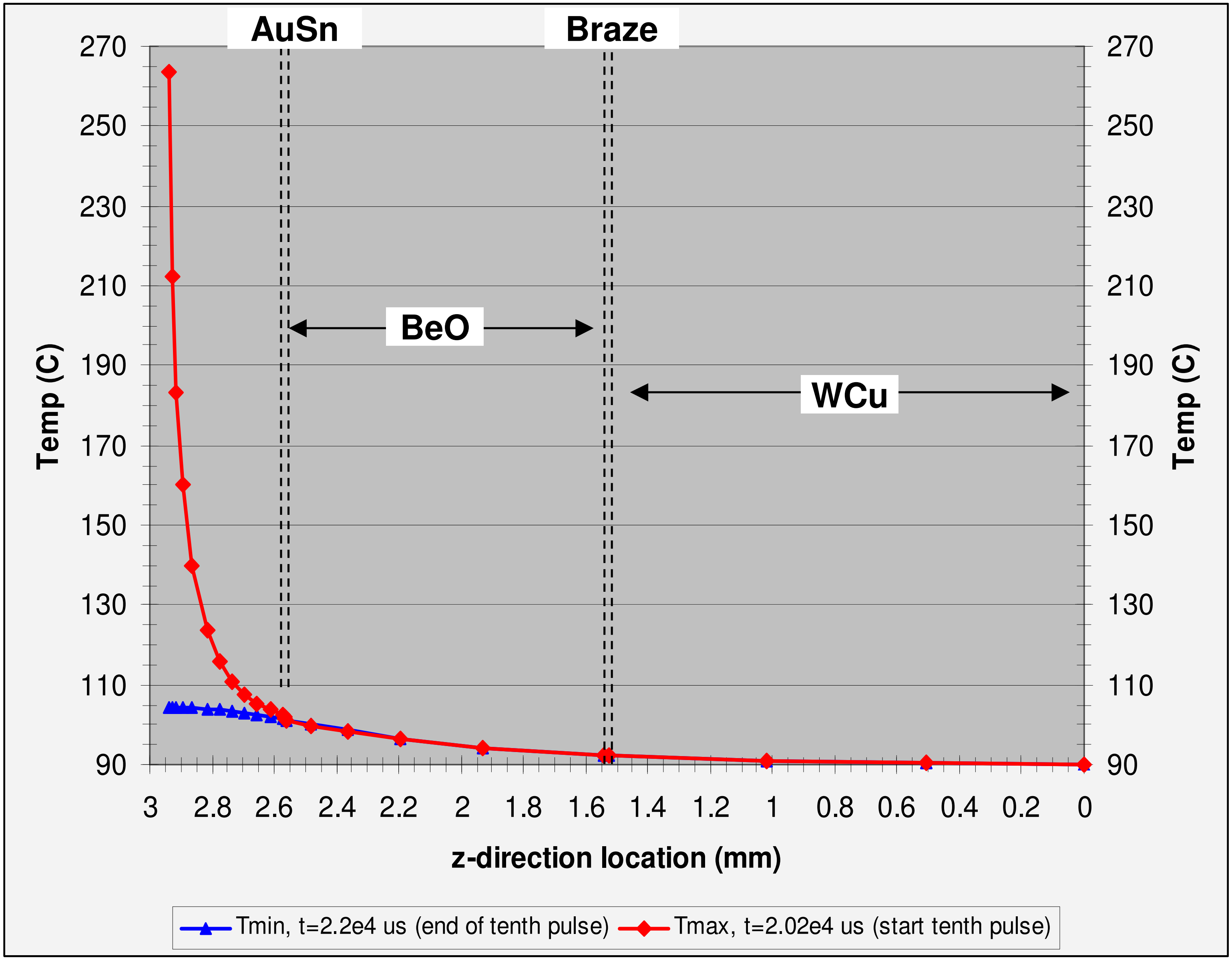
Image used to correlate with IR measurement

Sharp “spike-like” thermal gradients can be resolved with submodel technique



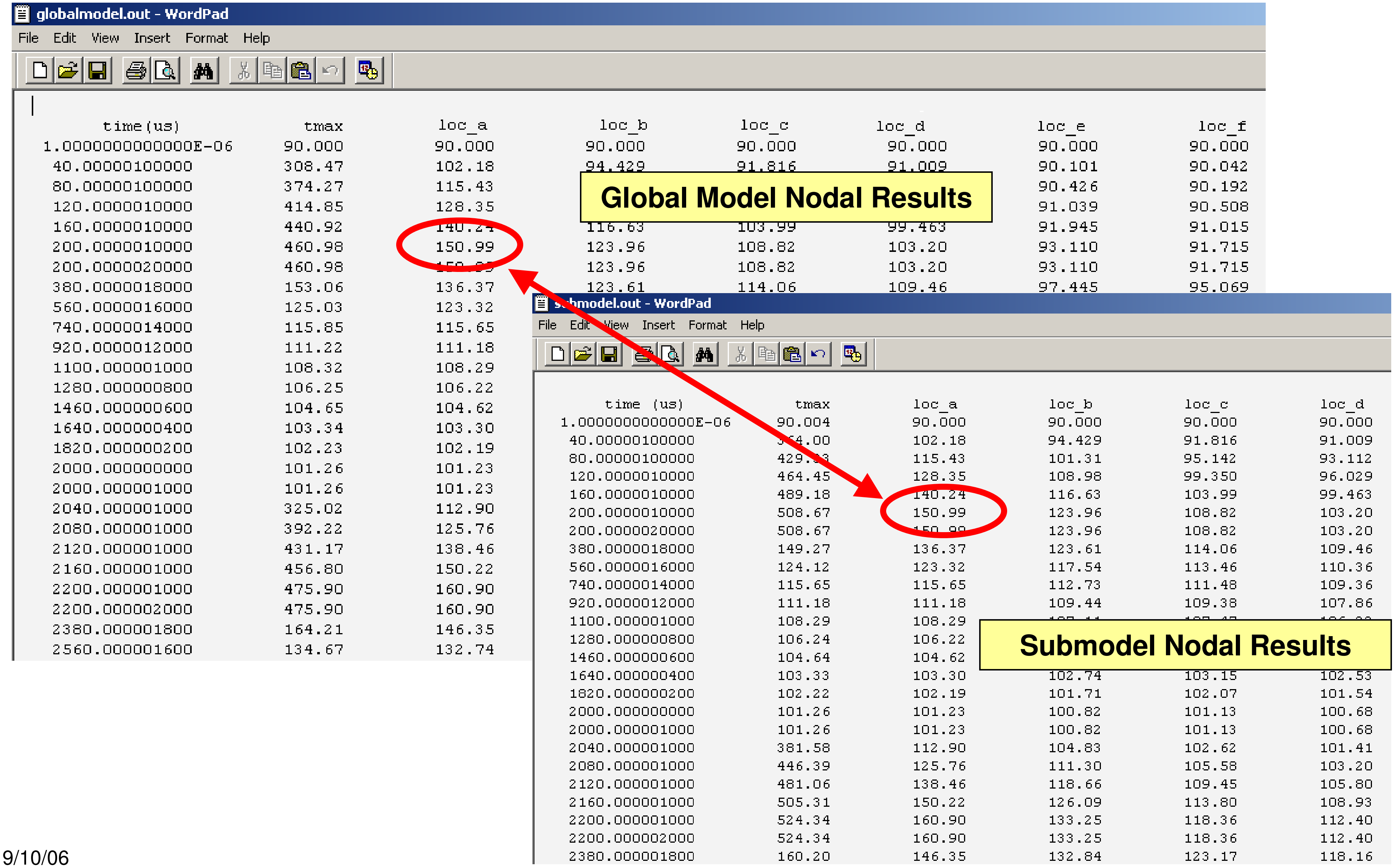
½ Symmetric Submodel 3D Temperature Plot.

Key Concept: Most Temperature Rise in Device



ANSYS Model “Typical” Output

Key locations in FE global/submodel are tracked in the time domain



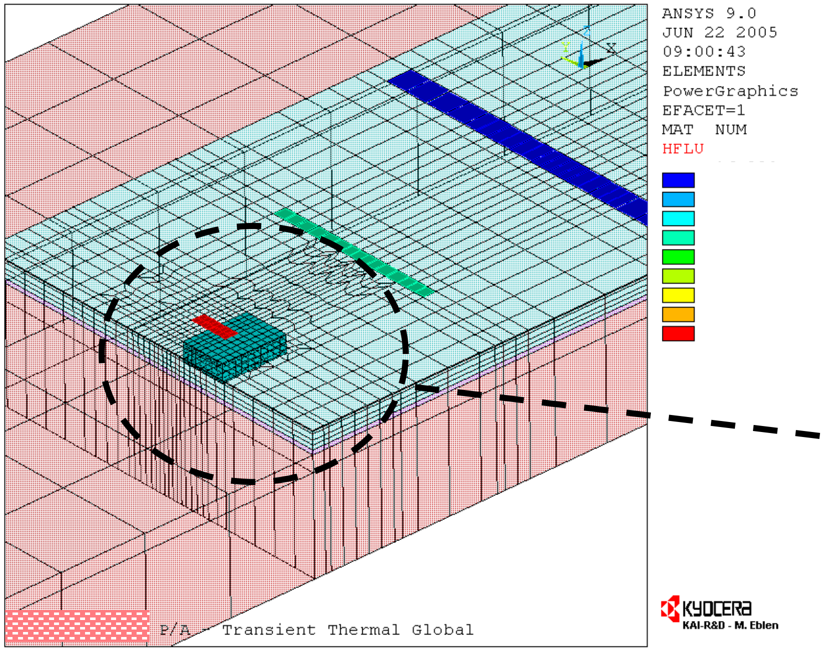
```
    time(us)              tmax         loc_a         loc_b         loc_c         loc_d         loc_e         loc_f
1.0000000000000E-06      90.000        90.000        90.000        90.000        90.000        90.000        90.000
 40.00000100000          308.47        102.18        94.429        91.816        91.009        90.101        90.042
 80.00000100000          374.27        115.43                                                  90.426        90.192
 120.0000010000          414.85        128.35                                                  91.039        90.508
 160.0000010000          440.92        140.24        116.63        103.99        99.463        91.945        91.015
 200.0000010000          460.98        150.99        123.96        108.82        103.20        93.110        91.715
 200.0000020000          460.98        150.99        123.96        108.82        103.20        93.110        91.715
 380.0000018000          153.06        136.37        123.61        114.06        109.46        97.445        95.069
 560.0000016000          125.03        123.32
 740.0000014000          115.85        115.65
 920.0000012000          111.22        111.18
 1100.000001000          108.32        108.29
 1280.000000800          106.25        106.22
 1460.000000600          104.65        104.62
 1640.000000400          103.34        103.30
 1820.000000200          102.23        102.19
 2000.000000000          101.26        101.23
 2000.000001000          101.26        101.23
 2040.000001000          325.02        112.90
 2080.000001000          392.22        125.76
 2120.000001000          431.17        138.46
 2160.000001000          456.80        150.22
 2200.000001000          475.90        160.90
 2200.000002000          475.90        160.90
 2380.000001800          164.21        146.35
 2560.000001600          134.67        132.74
```

Global Model Nodal Results

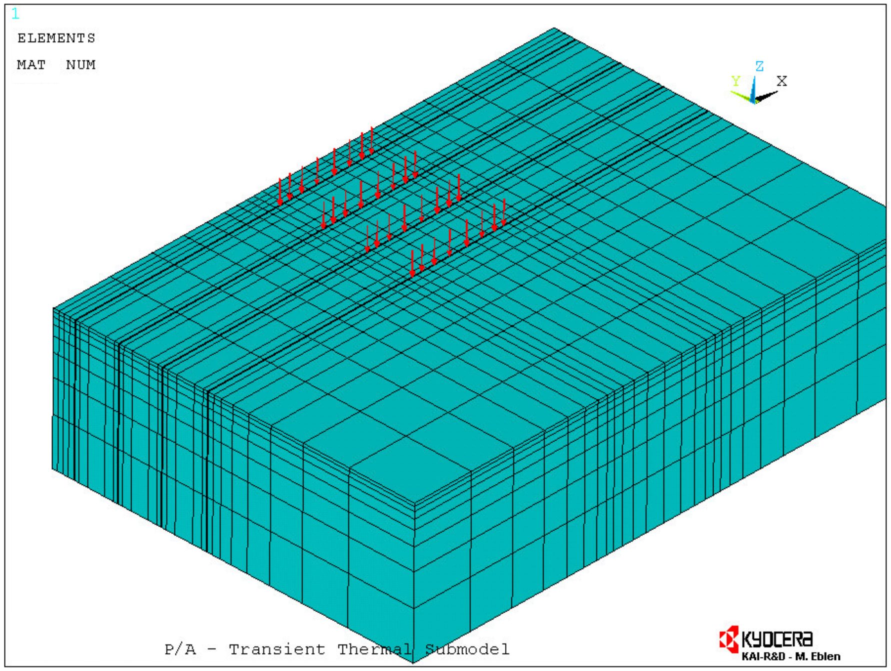
```
     time  (us)            tmax        loc_a        loc_b        loc_c        loc_d
1.0000000000000E-06       90.004       90.000       90.000       90.000       90.000
 40.00000100000           364.00       102.18       94.429       91.816       91.009
 80.00000100000           429.[illegible]3 115.43    101.31       95.142       93.112
 120.0000010000           464.45       128.35       108.98       99.350       96.029
 160.0000010000           489.18       140.24       116.63       103.99       99.463
 200.0000010000           508.67       150.99       123.96       108.82       103.20
 200.0000020000           508.67       150.99       123.96       108.82       103.20
 380.0000018000           149.27       136.37       123.61       114.06       109.46
 560.0000016000           124.12       123.32       117.54       113.46       110.36
 740.0000014000           115.65       115.65       112.73       111.48       109.36
 920.0000012000           111.18       111.18       109.44       109.38       107.86
 1100.000001000           108.29       108.29
 1280.000000800           106.24       106.22
 1460.000000600           104.64       104.62
 1640.000000400           103.33       103.30       102.74       103.15       102.53
 1820.000000200           102.22       102.19       101.71       102.07       101.54
 2000.000000000           101.26       101.23       100.82       101.13       100.68
 2000.000001000           101.26       101.23       100.82       101.13       100.68
 2040.000001000           381.58       112.90       104.83       102.62       101.41
 2080.000001000           446.39       125.76       111.30       105.58       103.20
 2120.000001000           481.06       138.46       118.66       109.45       105.80
 2160.000001000           505.31       150.22       126.09       113.80       108.93
 2200.000001000           524.34       160.90       133.25       118.36       112.40
 2200.000002000           524.34       160.90       133.25       118.36       112.40
 2380.000001800           160.20       146.35       132.84       123.17       118.16
```

Submodel Nodal Results

FE Submodel Technique Also Used for GaAs FETs

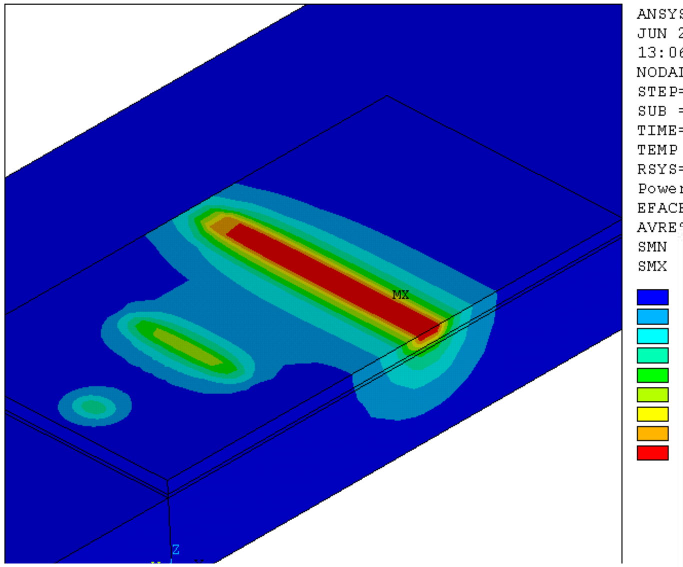


Course mesh global model with ½ symmetric submodel volume shaded. Note: constraint equations were used to tie h/s course mesh with GaAs fine mesh.



Detailed view of ½ symmetric submodel. Thermal bc's specified on all surfaces except top face.

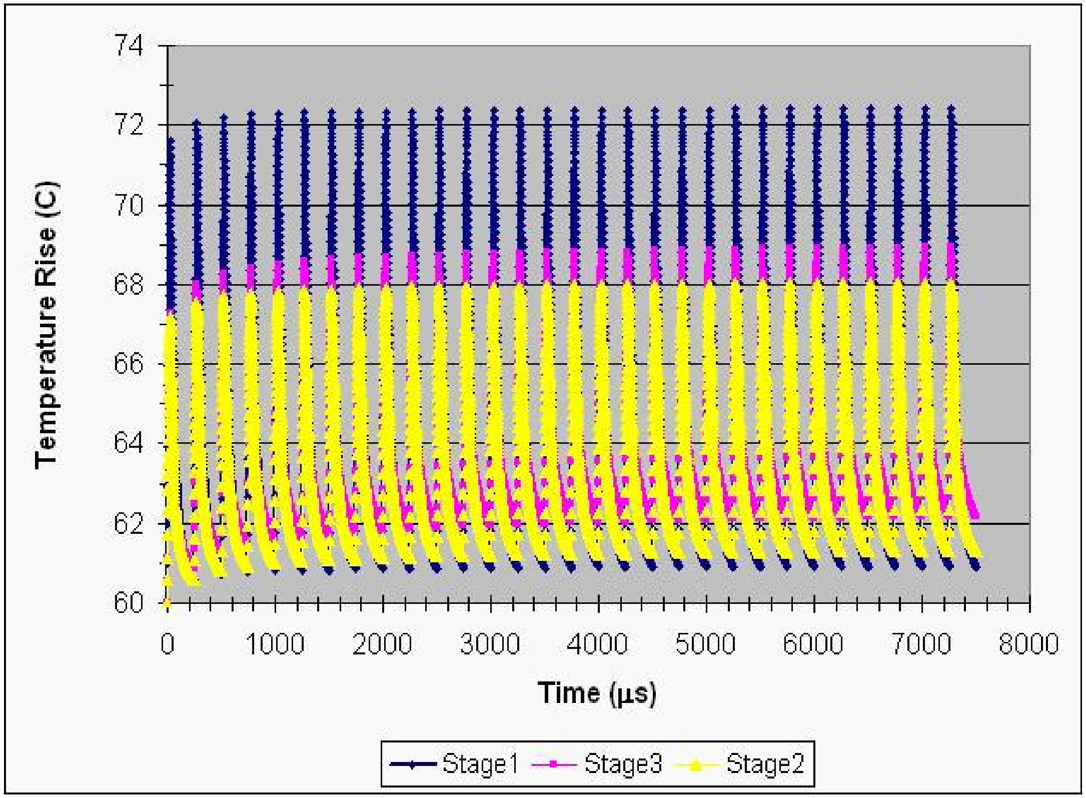
AuSn Solder Die Attach Transient Thermal FE Results



```
ANSYS 9.0
JUN 24 2005
13:06:26
NODAL SOLUTION
STEP=124
SUB =5
TIME=.00775
TEMP      (AVG)
RSYS=0
PowerGraphics
EFACET=1
AVRES=Mat
SMN
SMX
```

Global Temp Plot During Pulse Off Conditions.

Very little capacitive thermal coupling between P/A stages (e.g. thermal diffusivity of all materials is high)



10% Duty Cycle Transient ΔT History for all P/A Stages.

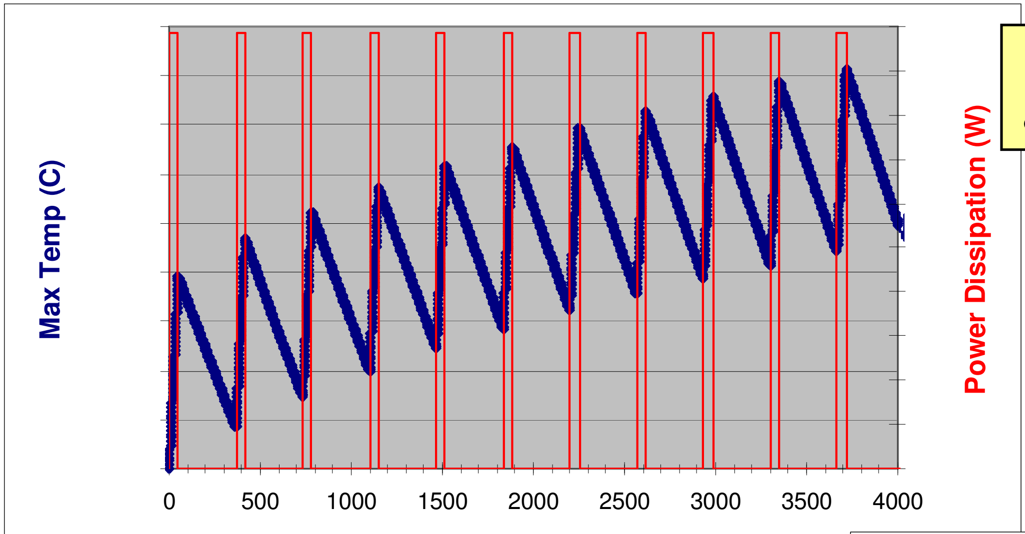
$$\alpha = \frac{k}{\rho \cdot c_p}$$

α = thermal diffusivity

k = thermal conductivity

ρc_p = volumetric heat capacity

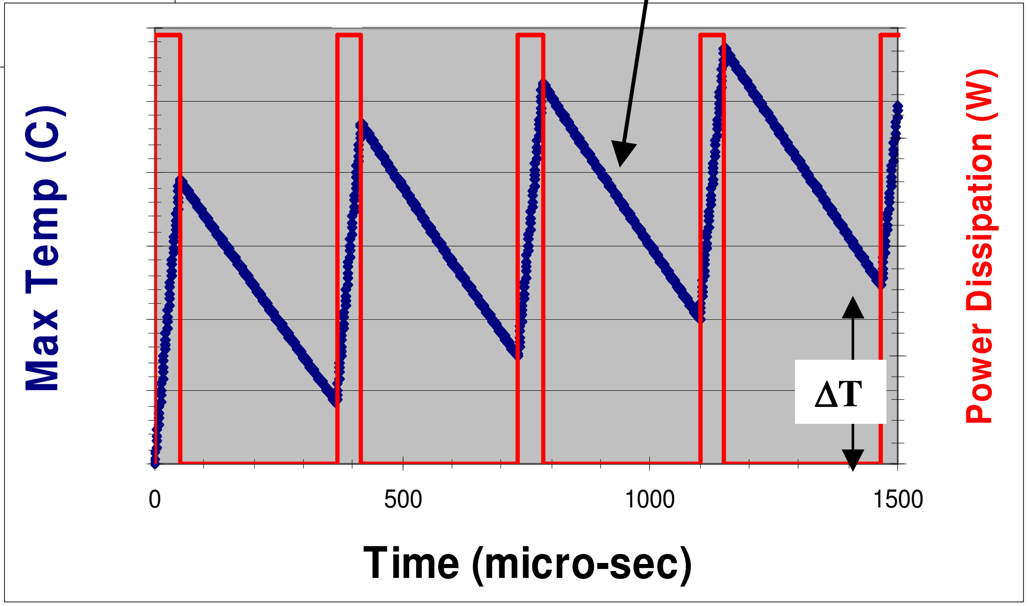
What if Scenario: Epoxy Die Attach



Eventual quasi-steady state temperature achieved after ≈ 8 sec

Transient ΔT History
(4mil epoxy @ k=2.0 W/mK)

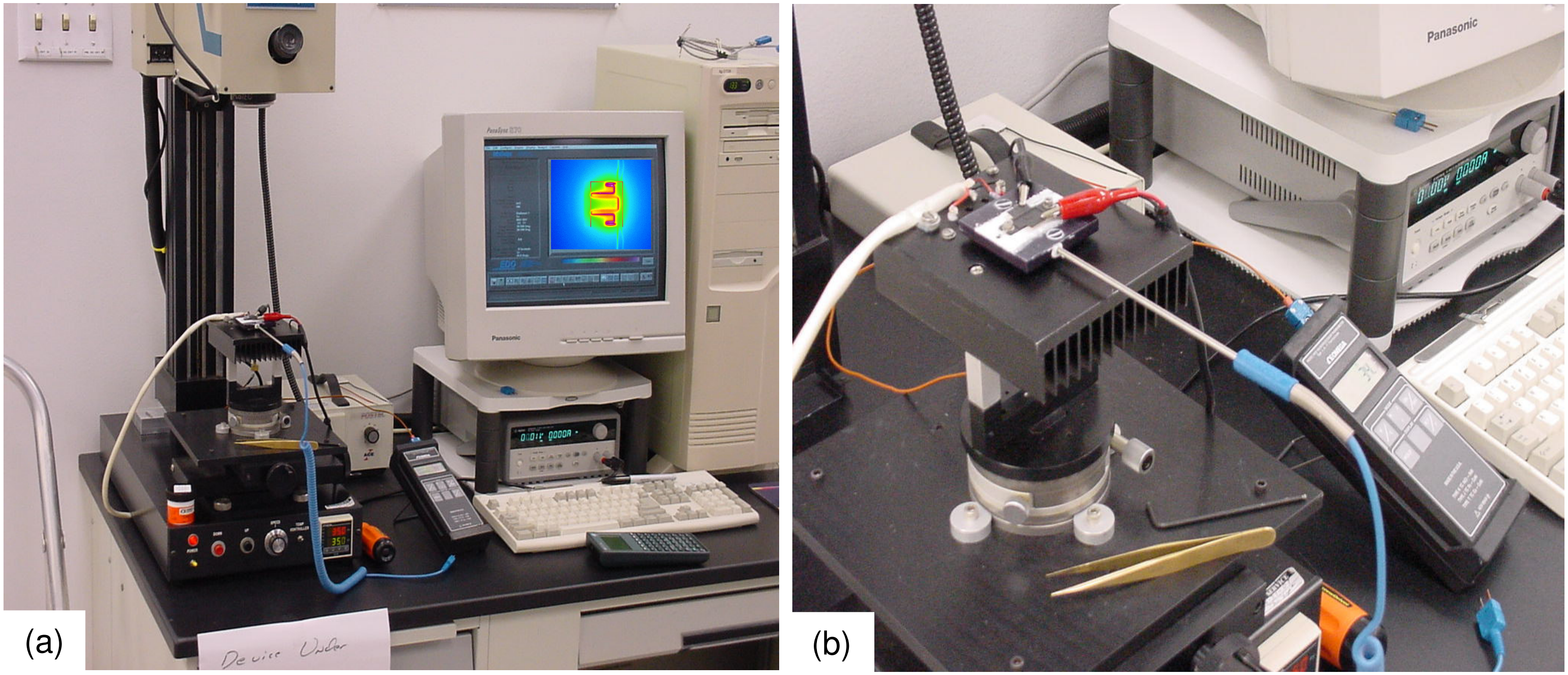
Monotonic sawtooth response due to poor thermal diffusion (ie low epoxy diffusivity)



Validation: KAI-R&D Internal θ_{jc} Measurements

Scope:

Conduct steady-state internal θ_{jc} measurements on laminate heat sink pkgs. The control group shall be a conventional CuW pkg in the same outline.

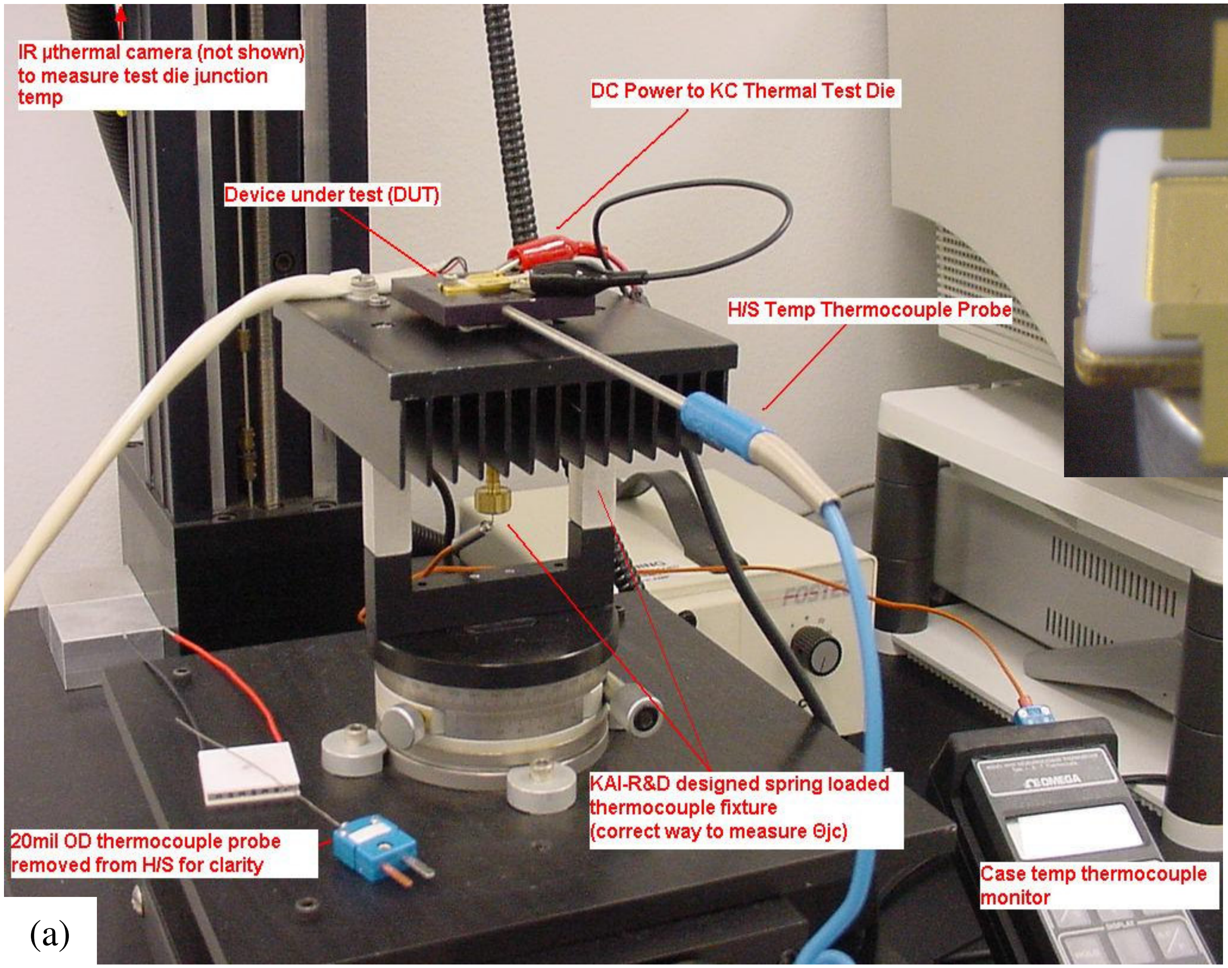


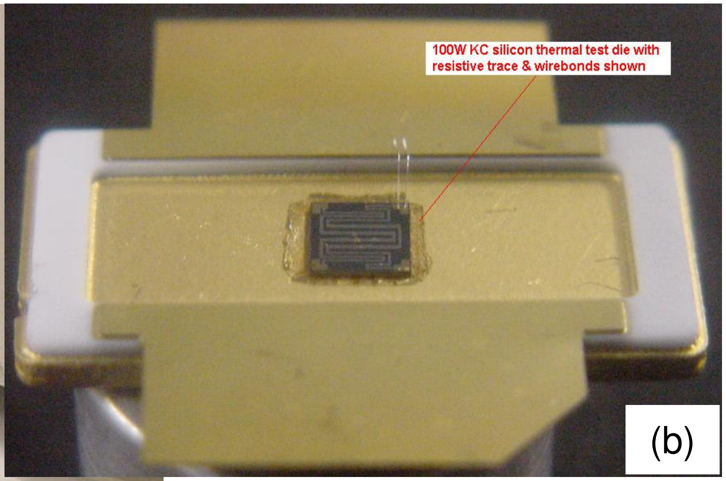
(a)

(b)

Fig. 1 (a) KAI-R&D infrared μthermal imaging system to measure package θ_{jc}. (b) Detailed view of package measurement setup showing sample coated with a fine layer of high emissivity paint for a reliable IR scan (*Note: Si is translucent at 5μm*).

θ_{jc} Measurement Setup Description





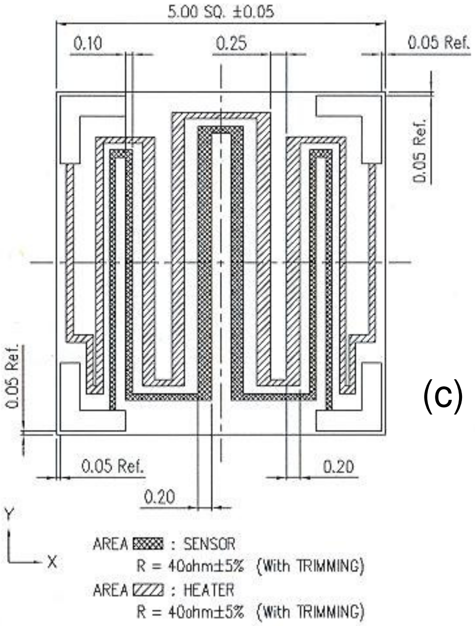
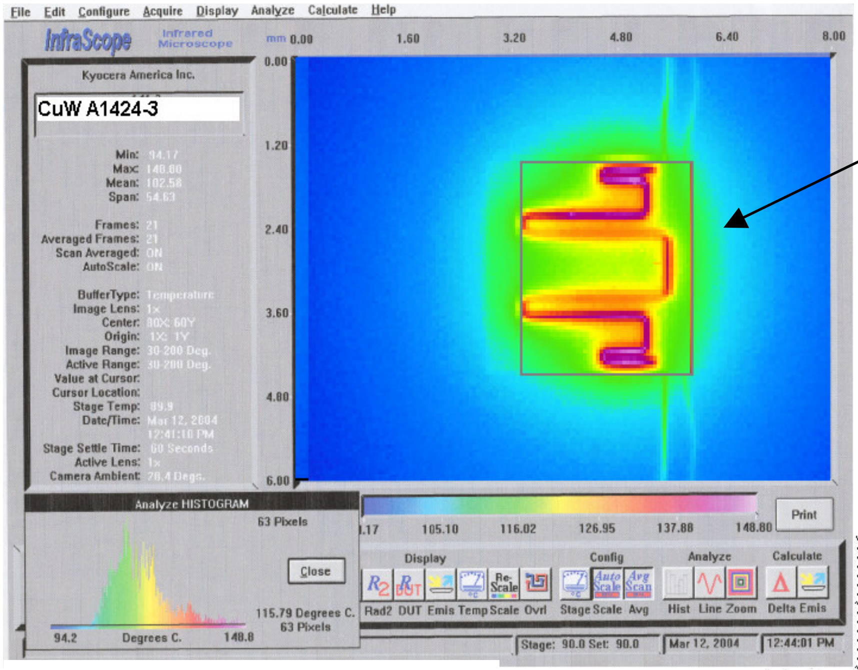


Fig 4: (a) Test setup with description. (b) A1670 package with thermal test die attached. (c) Kyocera 5 x 5 x .4mm 100W silicon thermal test chip dwg, illustrating RTD temperature sensor pattern and heater resistive pattern.

KYOCERA

Steady State IR Measurement Results cont…



Kyocera America Inc.

CuW A1424-3

Min: 94.17
Max: 148.80
Mean: 102.58
Span: 54.63

Frames: 21
Averaged Frames: 21
Scan Averaged: ON
AutoScale: ON

BufferType: Temperature
Image Lens: 1x
Center: 80X: 60Y
Origin: 1X: 1Y
Image Range: 30-200 Deg.
Active Range: 30-200 Deg.
Value at Cursor:
Cursor Location:
Stage Temp: 89.9
Date/Time: Mar 12, 2004 12:41:10 PM
Stage Settle Time: 60 Seconds
Active Lens: 1x
Camera Ambient: 28.4 Degs.

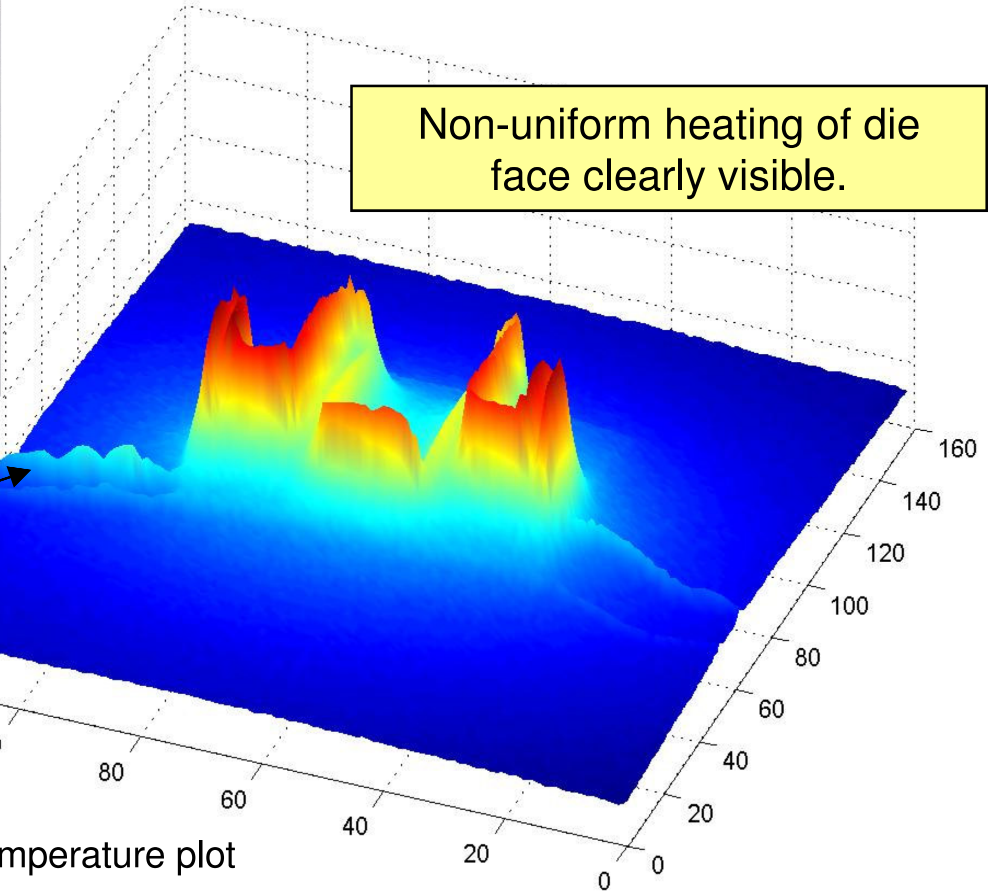
63 Pixels

115.79 Degrees C.
63 Pixels

Stage: 90.0 Set: 90.0
Mar 12, 2004
12:44:01 PM

InfraScope™ GUI

Average temperature for area was taken as T_j, refer to histogram bottom left.



Non-uniform heating of die face clearly visible.

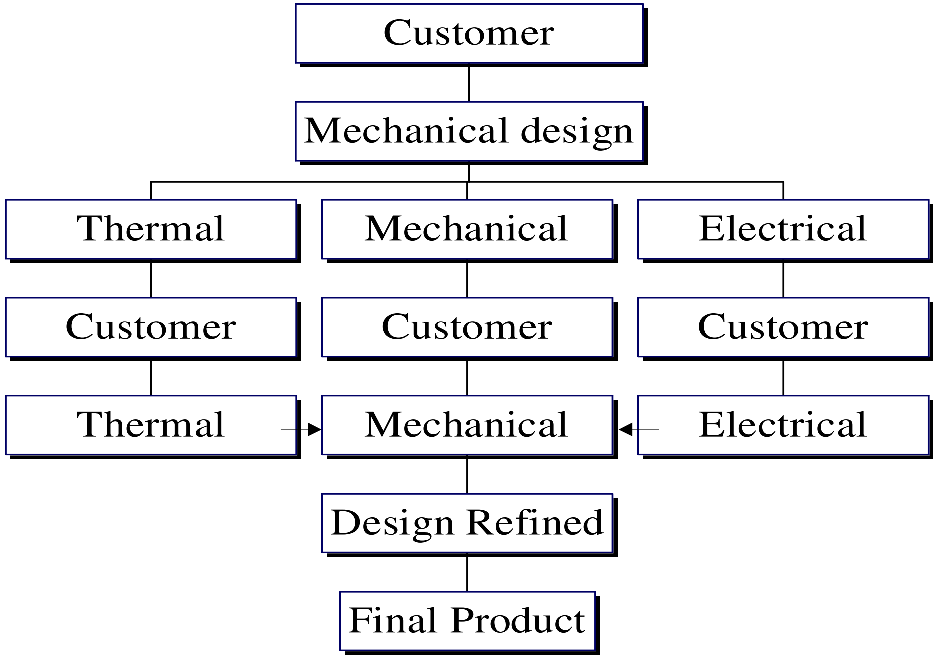
wirebonds

3D temperature plot

9/10/06

Conclusions

- Thermal behavior of WBG devices can be effectively modeled using standard FE tools. Careful understanding of boundary conditions is critical.
- Must characterize thermophysical materials over temperature of interest.
- Should include device transistor details in thermal model. Majority of temperature rise is in top layers of device.
- Validate thermal model assumptions via IR imaging in time domain (TBD).
- Thermal design is one part of a integrated design approach.



Appendix

Fundamental Concepts - Continued

The thermal interface resistance across a joint is a complex function of the geometric and thermophysical properties of the contacting solids and of any interstitial substance at the interface(ie air or thermal grease). The important parameters are: surface texture, waviness, hardness, modulus of elasticity, mechanical load, temperature levels, and material conductivity's.

(refs: Incropera & Dewitt, M. M. Yovanovich - MHTL Waterloo)

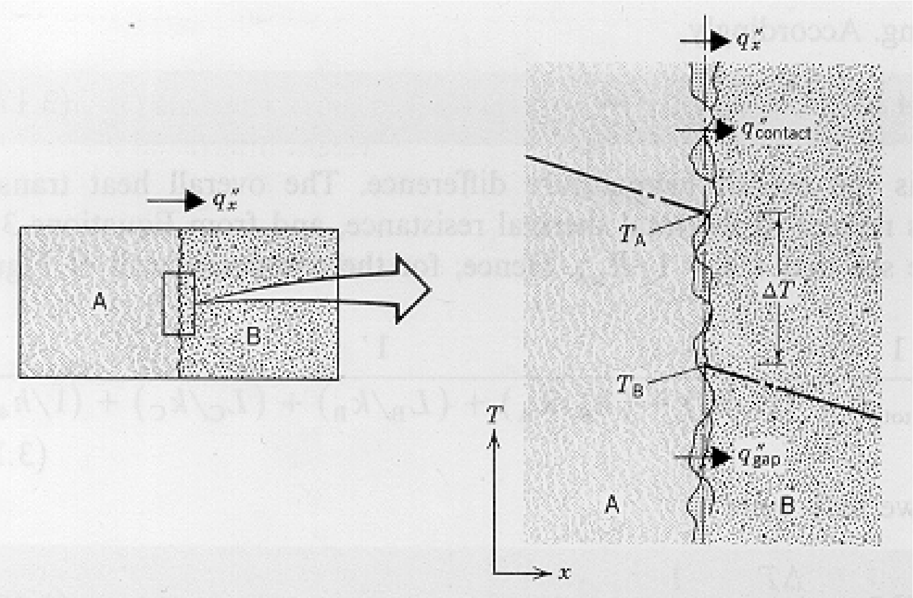
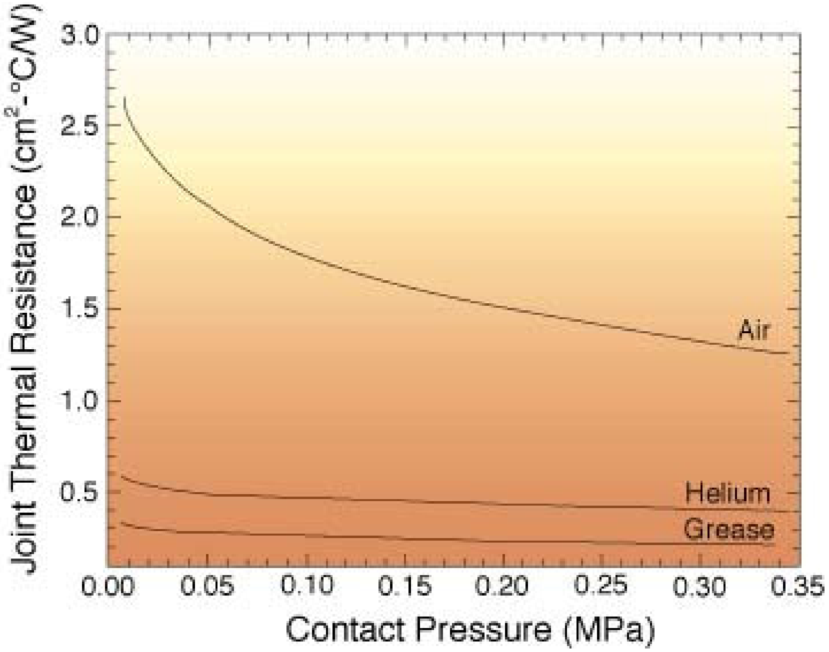


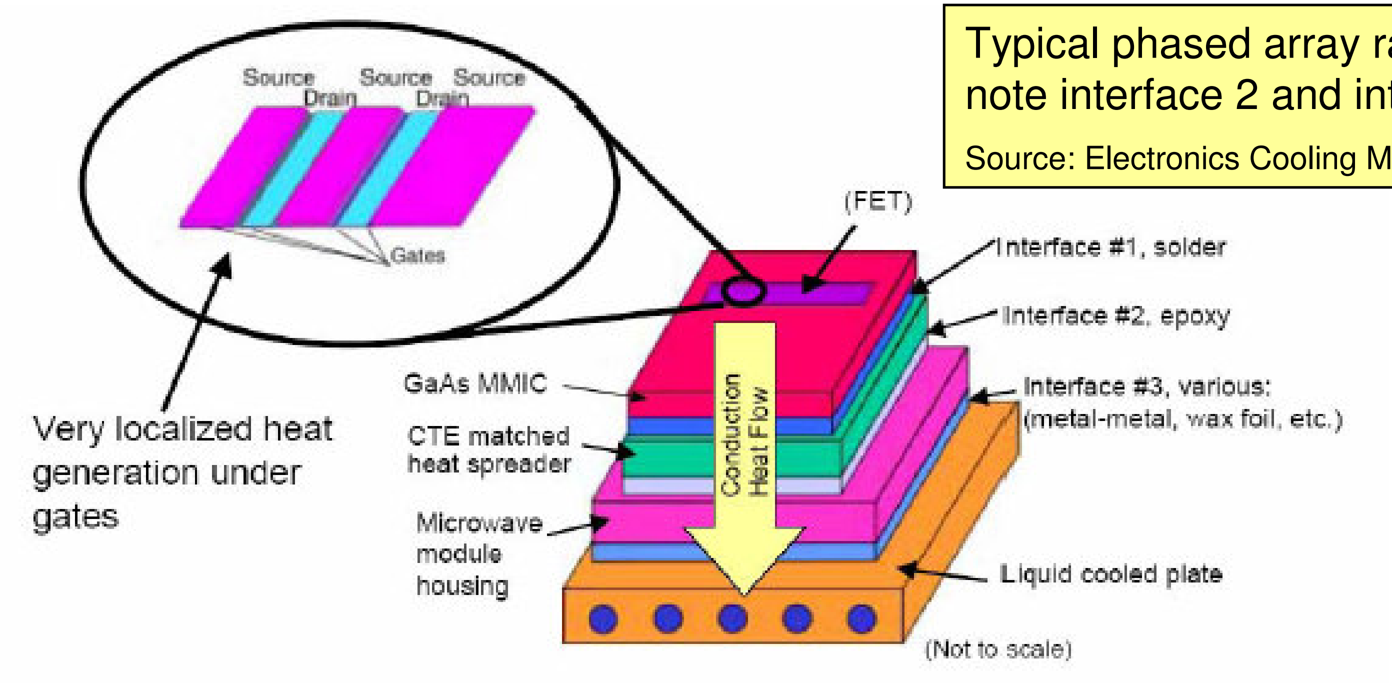
Figure 3.4 Temperature drop due to thermal contact resistance.



Cooling Strategy Will Be Critical!

Typical phased array radar conduction path, note interface 2 and interface 3.

Source: Electronics Cooling Magazine - Jim Wilson Raytheon.



Example of liquid cooling of chip face