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LTCC DIVISION OF KYOCERA AMERICA DESIGN GUIDE

- ♦ HIGH RELIABILITY
- ♦ HIGH INTERCONNECT DENSITY
- ♦ HIGH I/O COUNT
- ♦ EXCELLENT POWER HANDLING
- ♦ LOW-FIRE MATERIAL
- ♦ CUSTOM TRANSMISSION LINES
- ♦ CUSTOM MULTICHIP MODULES
- ♦ EMBEDDED PASSIVE COMPONENTS

Kyocera America
LTCC Division
March 2004

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LTCC Design Guide

Multilayer Ceramic (MLC) Devices offer an alternative packaging method for thin and thick film hybrids, plastic packages, etched circuit boards and other packaging methods. MLC offers innovative technical solutions with extensive design options with low NRE and fast deliveries. New low fire processes utilizing noble metal conductors, known as LTCC, offer significant performance opportunities. KAI LTCC uses low dielectric tapes manufactured by Dupont and Ferro. All material systems are supported with gold and silver conductor materials. A full range of components (e.g., seal rings, pins, R.F. connectors and heat sinks) can be brazed with gold-based brazes, or soldered with lead-based solders. All tape systems offer a full range of resistor materials that can be co-fired with the tape on the surface for laser trimming to high tolerances or on internal layers for devices such as voltage dividers.

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Production Processes

Kyocera America's LTCC division is capable of producing parts in high volume or in prototype lots. The design considerations of each style of production are different. High volume manufacturing requires maximizing through-put, while minimizing the number of operations in order to minimize cost. These considerations require tolerances to be increased while the number of via sizes or features (such as cavities) should be minimized.

The LTCC division is also the premier producer of complex LTCC packages. These packages are typically manufactured in low volume, and require very tight tolerances. To accommodate both needs, this design guide presents two levels of tolerancing to follow: the "preferred" tolerancing is required for high volume manufacturing. The minimum tolerancing can be accommodated at low volume manufacturing, but will entail a higher cost.

For either high or low volume, the quote and production process is the same, and is illustrated below. Paramount to the process is interaction with the customer at quote generation, contract review, and project review. These interactions ensure that what is produced and delivered is exactly what the customer wants and needs.

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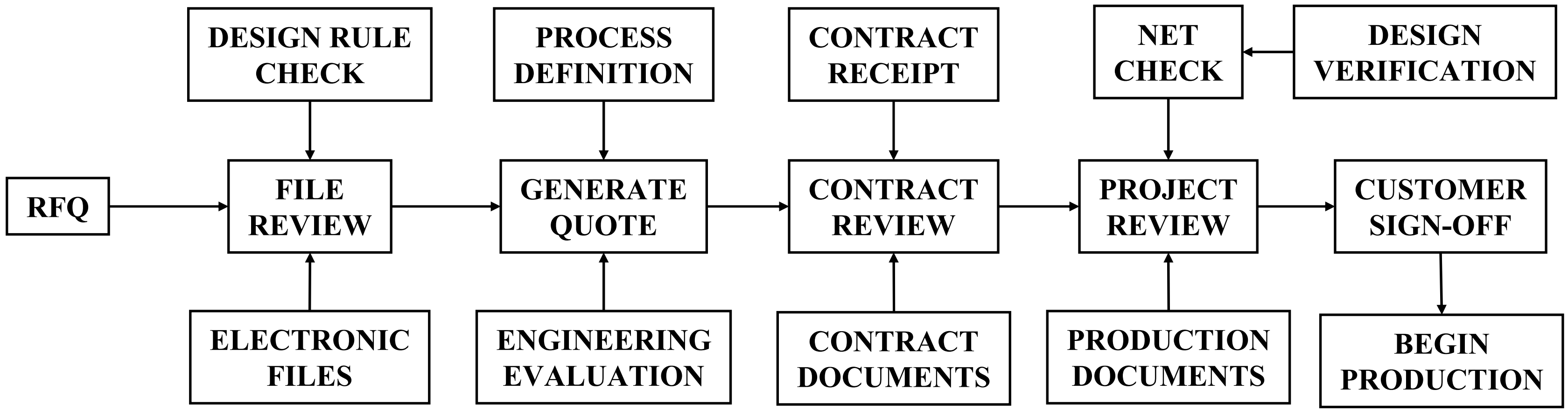
Production Processes



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Materials and Properties

Material Property	units	Dupont 951	Dupont 943	Ferro A6M	Ferro A6S
ELECTRICAL					
Dielectric Constant	(0.1-2 GHz)	7.8	7.4	5.9	5.9
Dielectric Loss Factor	(0.1-2 GHz)	0.0015	0.0005	0.0012	0.0012
THERMAL					
Expansion Coefficient	(ppm/C)	5.8	6	7	>8
Conductivity	(W/mK)	3.3	4.4	2	2
MECHANICAL					
Flexural Strength	(MPa)	320	230	170	>160
Young's Modulus	(GPa)	120	150	92	92
PHYSICAL					
Green Tape Thickness	(mils)	4.5, 6.5, 10	2, 5, 10	5, 10	5, 10
Fired Tape Thickness	(mils)	3.6, 5.4, 8.1	1.8, 4.5, 9	3.7, 7.4	3.9, 7.8

Process Variation

Kyocera LTCC is a data-oriented company, enabling the delivery of quality products our customers demand. All of our design criteria are based on extensive measurements of our processes, and defined as ± 3 standard deviations of the distribution.

SV: Shrinkage Variation = 3 sigma of fired length. It is critical to consider the impact of shrinkage variation on design considerations. Shrinkage behavior of ceramics depends on many parameters including particle size and shape distribution, as well as size and mass of the package laminate.

SV, Dupont 951 = 0.4% of linear dimension

SV, Ferro A6M = 0.9% of linear dimension

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Package Design Considerations

1. Maximum working area:
   - Ferro: 4.0in X 4.0in
   - Dupont: 4.30in X 4.30in
2. Minimum package thickness: .020in.
3. Avoid using thin tape (.0037 fired) for surface layers when defining layer stack.
4. When calculating overall package thickness, .0004in should be added to each tape layer containing greater than 30% metal coverage to compensate for metal loading.
5. Conductor layout of each tape layer should be uniform in X, Y and Z to minimize ceramic distortion caused by imbalanced metal loading.
6. Chamfered corners are acceptable, but not preferred. If chamfers are required, make reference or minimum tolerance of ±.010in to apply.
7. Standard dimensional tolerance of material is ±SV, No Less Than(NLT) ±.005in.
8. Standard flatness of .004in/in.

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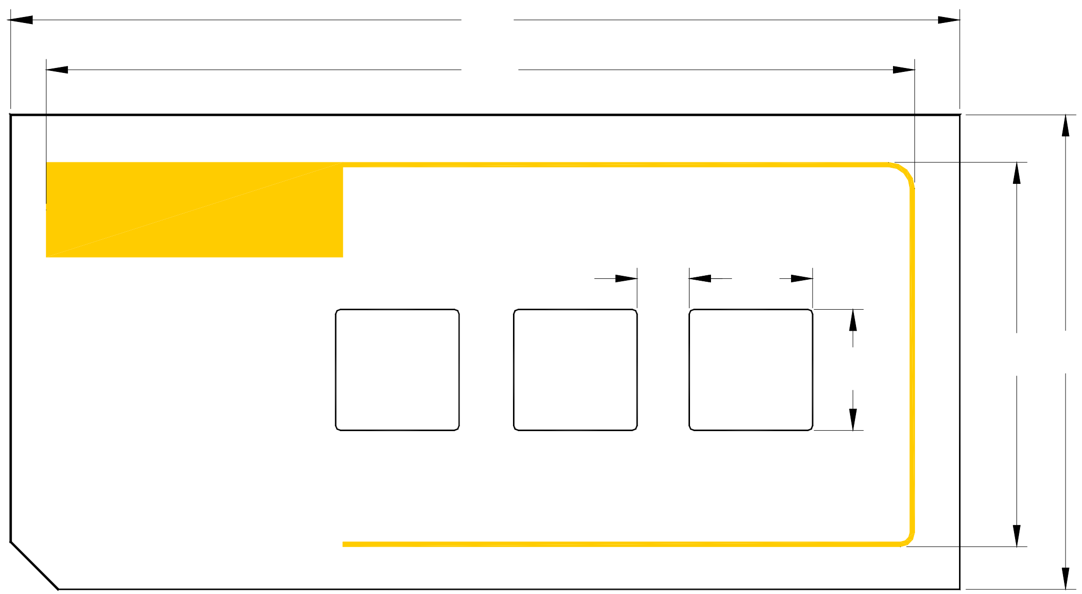
Package Design Considerations (cont.)

- X1 and Y1: Tolerances are defined by the cutting tolerance (typically ±.005”).
- X2 and Y2: Tolerances are defined by the material shrink variation. To prevent cutting into a conductor line, conductors must be pulled back a minimum of the shrink variation expected over the package length X1.
- X3 and Y3: Tolerances are defined by the shrink variation, with a minimum tolerance of ±.005in.
- X4: Width is a function of the number of cavities, package thickness, and Y3. Typically X4/Y3 minimum is 1/4.



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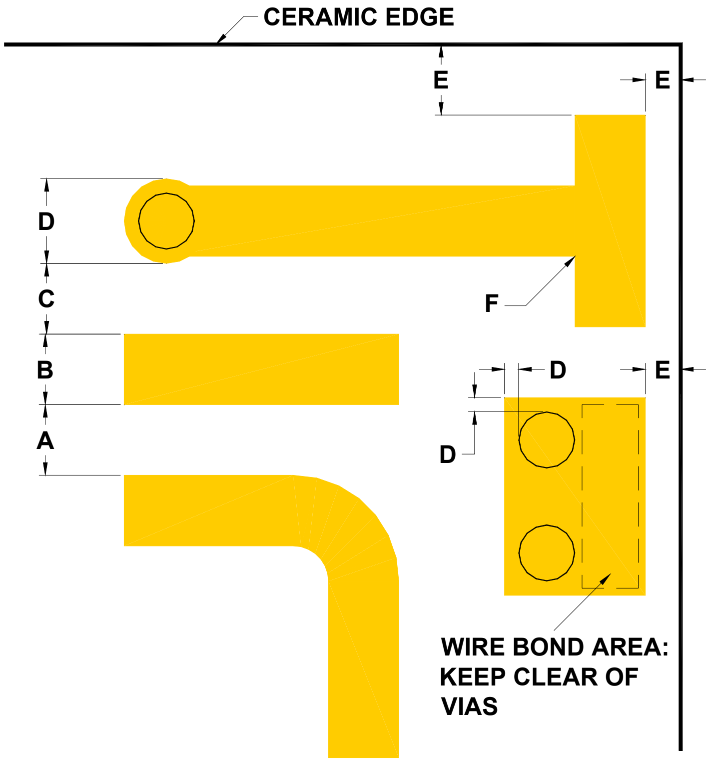
Conductors

Conductors are typically printed in the green (non-fired) stage on both exposed surfaces and/or buried tape layers. Conductor printing can be performed on fired tape (see later section for fired tape post printing) to the top and bottom most surface tape layer only. After firing, the conductors shrink to the specified length and width, but vary in both dimensions by the shrinkage tolerance. When placing conductors near ceramic edges, shrinkage variation must be considered to prevent cutting of the conductor unless internal exposed edge metallization (e.g. grounds) is acceptable.

Description		Preferred	Minimum
		(inch)	(inch)
A	Line Spaces	0.006	0.004
B	Line Width	0.006	0.004
C	Pad-to-Line	0.006	0.004
D	Cover Pad Dia.	Via dia.+0.004	Via dia.+0.002 **
E	Edge-to-Conductor	SV + 0.010	SV *
F	Expect Rounding of Internal Corners.		
*	**May require cutting metal.**		
**	**Not acceptable on vias exposed to surface layers.**		

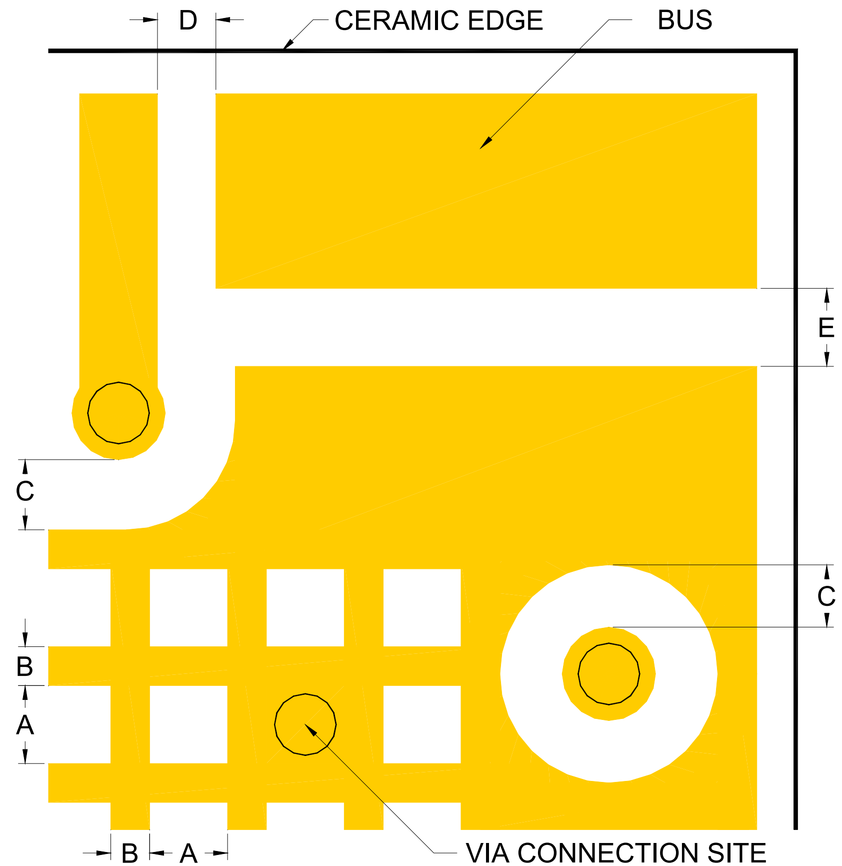


NOTE: Surface metallization may extend to ceramic edge, if conductor peeling, chipping and/or smearing at edge is acceptable.

Planes

Hatched planes are required internally or a hatch and solid combination is acceptable. Hatched planes use less gold, provide better tape-to-tape adhesion and create less ceramic distortion. Solid areas are required at plane via launch and land connection sites. Surface planes can be solid.

	Description	Preferred (inch)	Minimum (inch)
A	Grid Space	0.010	0.010
B	Grid Line	0.005	0.005
C	Via Catch Pad to Plane	0.012	0.008
D	Line-Plane/Bus *	0.010	0.008
E	Plane/Bus*-Plane/Bus *	0.012	0.010
*	**Bus is considered any conductor greater than .020in wide**		



NOTE: Standard rules for conductors apply.

Vias

Standard conductor rule applies for via capture pad. Via sizes are limited by tape thickness, due to aspect ratio of filling the vias. When selecting and placing vias the following rules should be considered:

- Maintain single via diameter throughout.
- Keep aspect ratio of via to tape as close to one (1) for optimum manufacturability.
- Stagger vias to reduce via posting at surface and if hermetic seal is required.

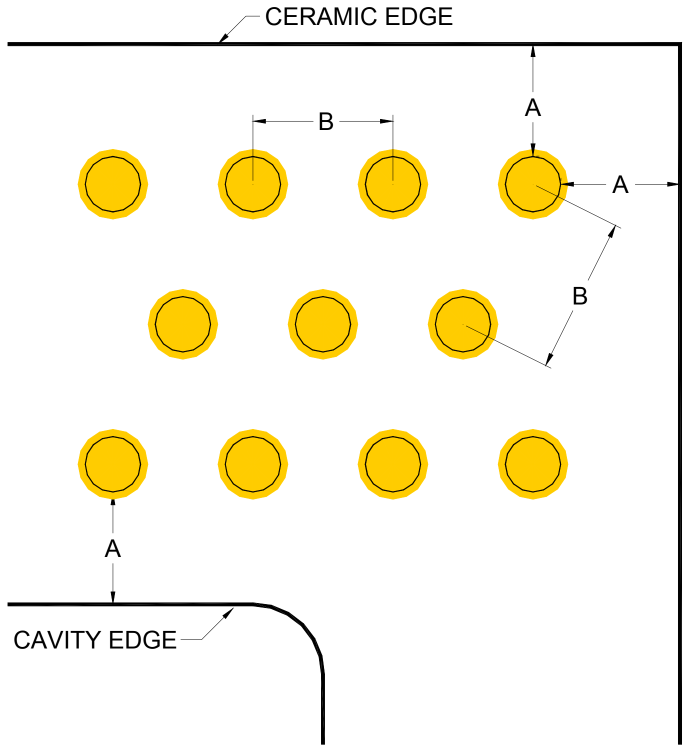
FIRED VIA SIZES			
FERRO A6M		DUPONT 951	
(inch)	(inch)	(inch)	(inch)
0.0037	0.0076	0.0039	0.0080
0.0046	0.0085	0.0048	0.0089
0.0050	0.0095	0.0052	0.0100
0.0056	0.0105	0.0059	0.0110
0.0066	0.0116	0.0069	0.0121

VIA TO TAPE SIZE		
Fired Tape Thickness	Preferred	Minimum
(inch)	(inch)	(inch)
< 0.004	0.006	0.004
> 0.004	0.008	0.006

Via Pitch

There are three (3) general types of vias: Rf-shield, thermal and signal. Signal vias are placed for optimization and do not typically follow any placement pattern. Thermal and RF-shield vias are usually placed in arrays within close proximity to each other. Via pitch is defined by the center line measurement from via to via. Via spacing is critical and all via types should follow rules outlined in table.

VIA TO VIA PITCH		
	Preferred	**Minimum**
A	SV + 0.010"	SV*
B	3 X dia.	2 X dia.**
*	**No less than .010in, may require cutting via.**	
**	**No less than .014in**	



NOTE: Thermal and RF-shield via arrays larger than .250 sq. should be avoided.

NOTE: Via castellations at ceramic edge are permissible with vendors approval.

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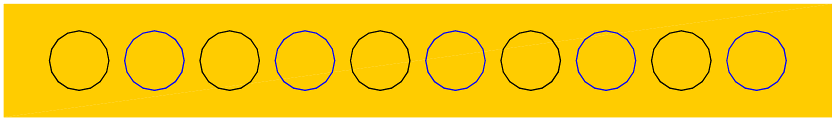
Via Stack

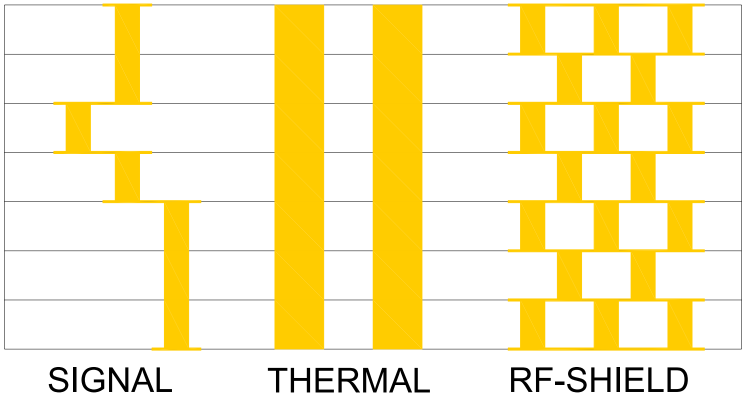
Via stacking should be avoided when possible. When it is necessary to stack vias, consideration should be given to the stack method defined for each configuration.

Illustration of the via types in cross-section:

- Signal - Random stagger with trace connecting launch and land by traces; cover pads required per standard conductor rule.
- Thermal - Typically require stack and larger via diameters of .008in to .012in. Cover pads for vias greater than .008in diameter are vendors option. Via posting will occur.
- RF-Shield-Staggered with conductor on each layer for electrical connection; cover pads required per standard conductor rule.



RF-Shield via layer to layer connection



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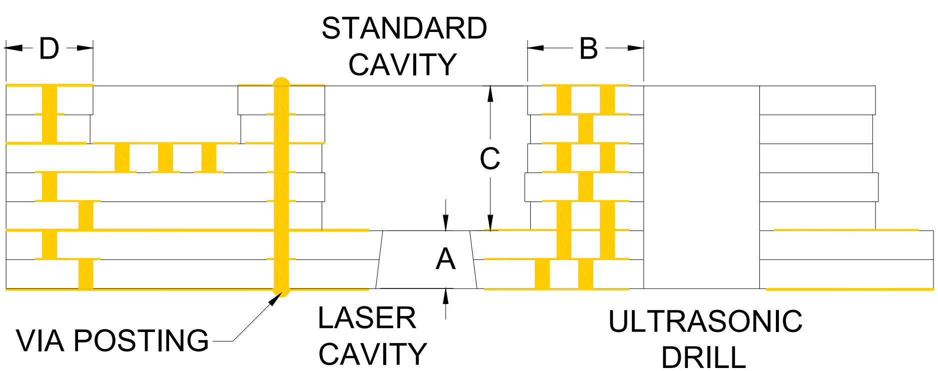
Cavity Design

Cavity size, shape and position are critical to manufacturing, performance and assembly. If improperly designed deformation of cavity walls may occur. Cavities can be formed using various methods each providing benefit at cost.

- Standard Punch: Most cost effective and shortest lead time, performed in-house. Cavity walls will display shift from adjacent layers. Used for all blind cavity generation.
- Laser Cut: Provides greater positional accuracy and tighter size tolerance at higher cost and longer lead time. Laser is limited to .070~.080in thick. Laser drilled cavities exhibit a 8% taper in cavity walls from top to bottom. Used for through cavities. Not performed in-house.
- Ultrasonic Drill: Most accurate for size and position. Typically limited to small cavities and mounting holes. Longest lead required and highest cost. Not performed in-house.



Description		Preferred (inch)	Minimum (inch)
A	Bond Shelf Thickness	0.040	0.020
B	Inner Cavity Wall Width	0.070	0.050 *
C	Inner Cavity Wall Height **	0.050	0.0074
D	Outer Cavity Wall Width	0.120	0.100
B/C D/C	Cavity to Wall Aspect Ratio	2	0.5
*	**If no brazing required to wall top surface.**		
**	**Maximum is defined by the B/C or D/C aspect ratio.**		

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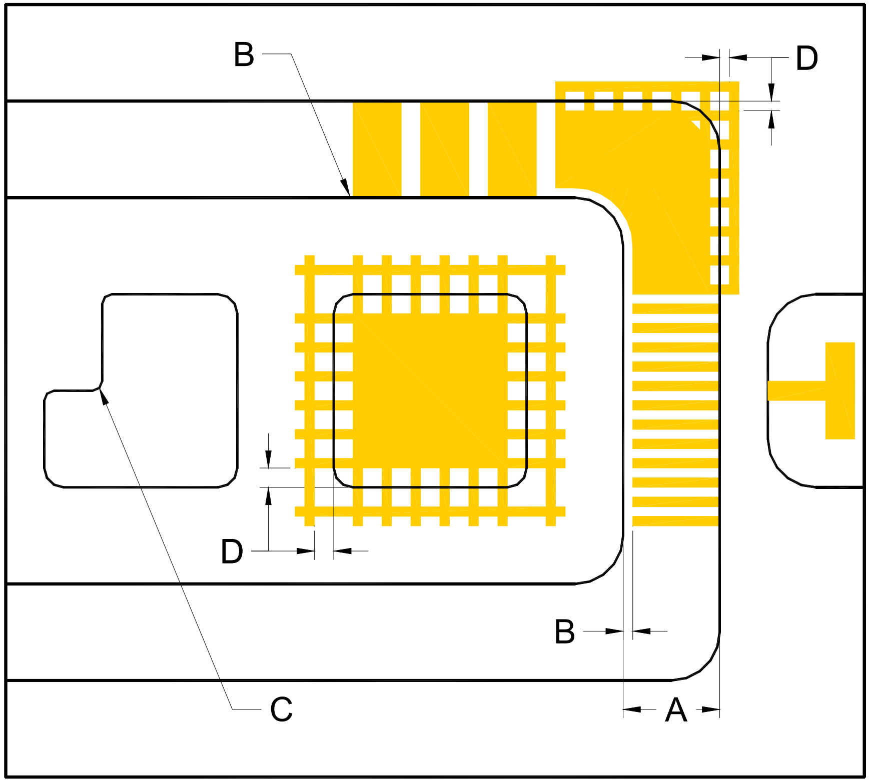
Cavity Rules

Conductors near or extending from cavities may cause deformation or delamination if improperly placed or patterned.

	Description	Preferred (inch)	Minimum (inch)
A	Bond Shelf Width	0.045	0.025 *
B	Conductor-to-Cavity Edge	0.005	0 **
C	Cavity Corner Radius	0.017	0.010
D	Conductor Under Cavity Transition ***	0.010/ SIDE	0.005/ SIDE
*	**Rounding of bond shelf edge may occur.**		
**	**May cause gold smear into cavity.**		
***	**Pads greater than .020in wide must be hatched prior to extending under cavity.**		



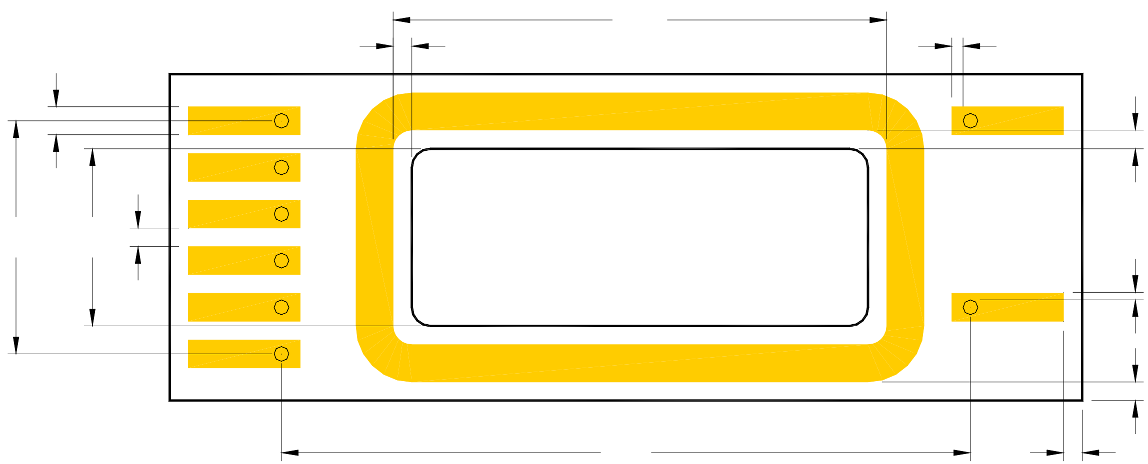
NOTE: Cavity outside corners will require radius.

NOTE: Standard conductor rules apply.

Post Print

Post printing refers to the process of printing conductors after firing the package, usually after cutting to size. This process is typically required for all brazing operations. It may also be used when final print dimension tolerances are tighter than the Shrinkage Variation. Post printing will also be required if grinding is necessary.

Description		Preferred (inch)	Minimum (inch)
A	Conductor to Part Edge	0.010	0.005
B	Conductor to Via Edge	SV of ½ X1 +0.010	+0.005
C	Conductor to Via Edge	SV of ½ Y1 +0.010	+0.005
D	Conductor to Cavity Edge	SV of ½ X2 +0.010	+0.005
E	Conductor to Cavity Edge	SV of ½ Y2 +0.010	+0.005
F	Conductor width or space	0.010	0.005



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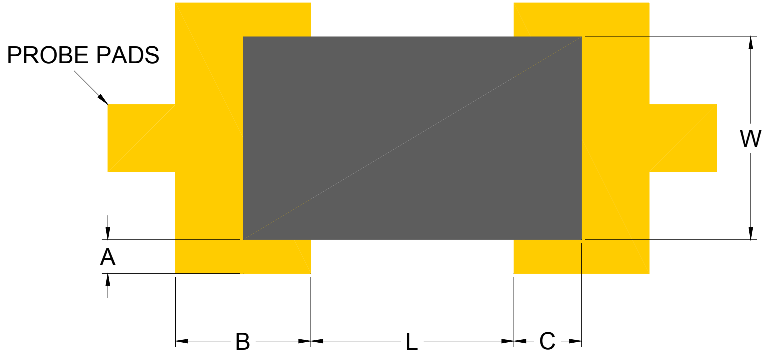
Cofired Resistors

Description		Preferred (inch)	Minimum (inch)
L	Resistor Length	0.025	0.015
W	Resistor Width	0.025	0.015
A	Termination Overhang	0.007	0.005
B	Termination Width	0.015	0.010
C	Resistor Overlap	0.010	0.007



Standard Decades
- 10 ohm
- 100 ohm
- 1 kohm
- 10 kohm
- 100 kohm (post fired Dupont only)
- 1 Mohm (post fired Dupont only)

$R = \rho * L / (W * T)$, ρ is resistivity of paste, T is resistor thickness

$R = \rho' * L/W$, ρ' is resistivity in ohms/square, L/W is # of squares

Tolerances
- Buried: +/- 30%
- Surface: Laser Trim to 2%*
  (*overglaze recommended)

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Cutting Processes

- Hot Knife: Least expensive. Ceramic X,Y outside dimension tolerance will be defined by Shrink Variation. **Not used on A6M**.
- Saw Cut: Provides best edge. Standard ceramic X,Y outside dimension tolerance of ±.005”.
- Laser Cut: Required for curved surfaces. Limited to .070~.080in thick. Laser cut will exhibit a 8% taper. Cutting through gold is not desired. Minimum scrap of 0.100” is required around cut line.
- Laser Scribe: Used for snapping small parts. Snap edge will exhibit roughness due to fracture.
- Hot Knife Scribe: Used for snapping small parts when ceramic X,Y outside dimension tolerance is not critical.

Developmental Processes

- Capacitors: Low values readily achieved by using tape as dielectric. Higher values possible using developmental pastes or tape with K of 20 (Dupont only). Implementation requires developmental efforts.

- Photoetch Conductors & Dielectrics: Currently used in development with customers. Line widths of 2 mil demonstrated.

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RF Simulation

The New Products Development (NPD) Group of Kyocera America, Inc. in San Diego has extensive experience modeling and verifying performance of LTCC packages. A variety of embedded elements have also been modeled and built, as part of a program to develop an embedded element library.

RF measurements are made with an HP 8510C Network Analyzer in conjunction with a CMT RF-1 probe station. Complex S-parameter measurements can be made at discrete frequencies, or the Time Domain Reflectometry capability yields impedance mismatch with respect to a 50 ohm system.

Electrical simulations can be carried out using Ansoft HFSS (frequency domain) or CST 3D FIT (time domain). These tools, in conjunction with physical parameter measurements, have been demonstrated to optimize performance and cost prior to building complex packages. Other software for simulation and optimization include Ansoft SPICE and Optimetrics, and UIUC Prime and 2D RLCG.

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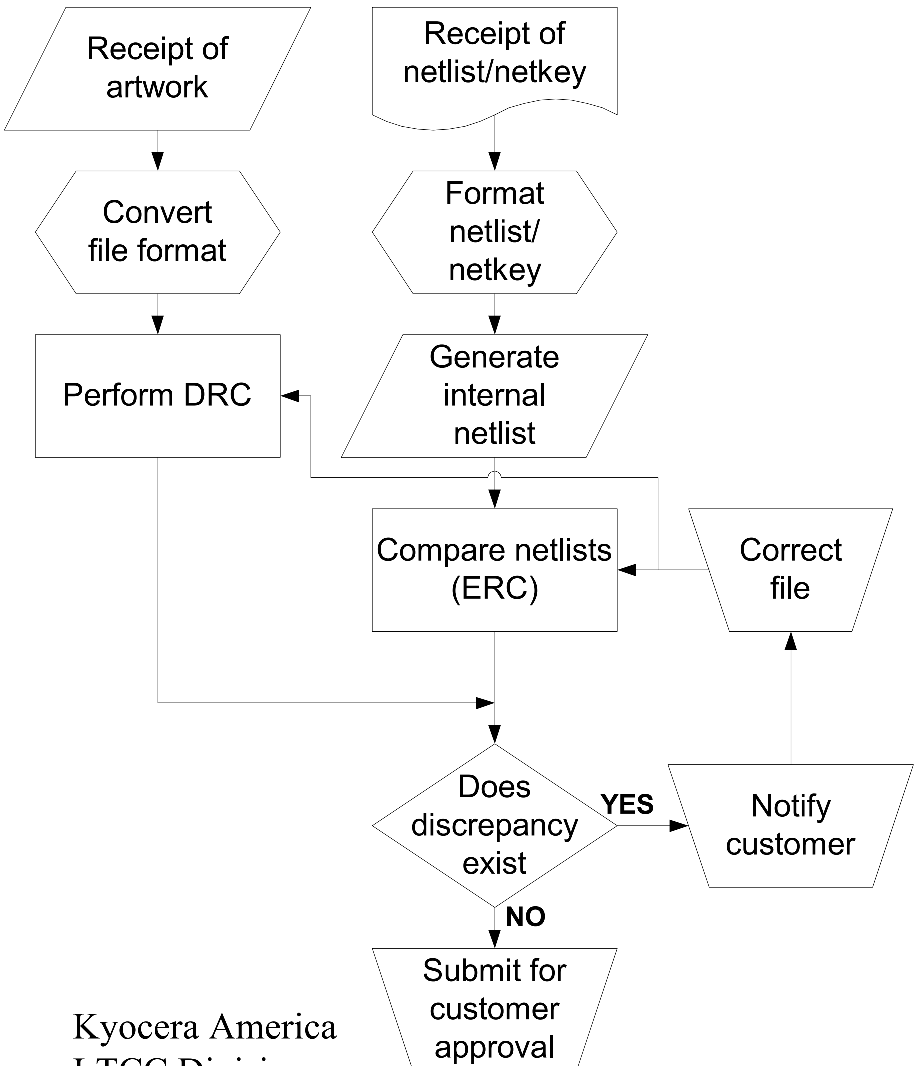
Design Verification Process



Electrical Rule Checking **(ERC)** and Design Rule Checking **(DRC)** are part of the design verification process.

• **ERC:** Verifyies the integrity of the data file received against the routing netlist.

• **DRC:** Verifyies the design layout meets manufacturing design rules as outlined within.

ARTWORK FILE FORMATS:

1) Gerber 274X w/embedded apertures.
2) Gerber 274D w/aperture list.
3) AutoCAD DWG format.
4) AutoCAD DXF format.

DRAWING FILE FORMATS:

1) AutoCAD DWG format.
2) AutoCAD DXF format.
3) ~.pdf
4) ~.bmp
5) Hardcopy

Design Verification Process (cont.)

Note: Netlist and Net Key are required for verification.

- NETLIST: The from-to list defining the routing connection path of each component pin. Typical format is as shown. Net names are not critical.
  - **File formats: 1) Excel spreadsheet 2) ASCII-word document 3) Schematic**
- NET KEY: Is the component footprint with reference designator, pin start, count and rotation. This is required for each component.
  - **File formats: 1) AutoCAD DWG/DXF 2) Gerber 274X 3) Hard copy**

NETLIST				
Net name	**Ref. Des/Pin number**			
$Net1	U8-1	U8-23	C1-1	JR-134
$Net2	U12-71	U5-171	U5-169	U5-173
$Net3	U5-158	U12-182	C1-2	
$Net4	U12-184	U5-186		
$Net5	U5-188	U5-194	U12-103	U12-115
*	U12-160	U5-196	JR-155	JT-197
*	U5-192	U5-198	U5-200	U5-202
$Net6	U12-162	JR-154		
$Net7	JT-189	U12-13