

# *A Propensity for Density*

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## *Introduction*

The "Need for Speed" for high-speed digital integrated circuits has created a demand for packages not only to serve as device attachment platforms, but as integral part of the circuit. The evolution of device miniaturization has created interfacing and attaching pad pitches well below 200 microns creating an upheaval in the packaging industry. Semiconductor manufacturers are not going to attach a device that is designed for flip chip attachment that can not even meet the device pad pitch. To meet this challenge, packaging manufacturers have developed very exotic and somewhat expensive technologies that were not industry acceptable for the market cost structure. However from this research, came developments and innovations meeting this device trend. The following discussion will address some of these developments.

## *Design Rules*

Flip chip technologies, while being over 30 years old, has made a major impact to the packaging industry. The de facto standard in the industry for years was based upon the IBM standards. These standards produced devices at pad pitches of 250 microns with line widths and spaces of 100 to 125 microns. This packaging technology was mainly confined within the walls of IBM. As IBM started to cross license their technology to the industry, there became an immediate need to develop packages with improved designed rules. Meanwhile ASIC and MPU companies were developing I/O counts rising faster than the chip area, and VLSI line geometry's are shrinking at faster rates than before. Today, every major semiconductor manufacturer has a flip chip program, whether this program is in full-scale

production, prototyping or in demonstration.

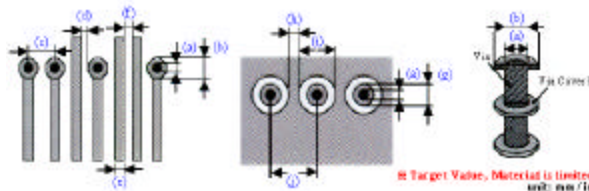
The first design rule improvement was to meet the current demand based upon the IBM standards. Packaging companies were able to meet this requirement by improving current manufacturing processes without sacrificing extensive investments. The next evolutionary step demanded more sophisticated manufacturing and/or post metalization techniques. The packaging industry went into a couple of directions.

One direction was to institute continue improvements on the current process. Depicted in the figure, is a table (Table 1) of design rules based upon the current manufacturing process. By improving material characterization and predicting precise multilayer ceramic shrinkage rates, packaging manufacturers were able to tighten the design rule demand to 50 micron geometry's, i.e. 50 micron

diameter via holes, lines and spaces at 150 micron pitches (CC050).

used extensively for high-end supercomputer and server packaging were cost is not as big of a factor as for consumer electronic equipment.

Pictured is a typical example of a high density surface mountable MPU package designed for flip chip attachment.



ITEM	CC000	CC100	CC075	CC050	CC030*
a). Via Hole Dia.	0.200 / 0.008"	0.100 / 0.004"	0.075 / 0.003"	0.050 / 0.002"	0.030 / 0.001"
b). Via Cover Dot Dia	0.381 / 0.015"	0.150 / 0.006"	0.127 / 0.005"	0.100 / 0.004"	0.050 / 0.002"
c). Via Center Spacing	0.635 / 0.025"	0.254 / 0.010"	0.200 / 0.008"	0.150 / 0.006"	0.080 / 0.0031"
d). Via Cover Dot to Line Clearance	0.254 / 0.010"	0.127 / 0.005"	0.075 / 0.003"	0.050 / 0.002"	0.030 / 0.001"
e). Line Width	0.127 / 0.005"	0.100 / 0.004"	0.075 / 0.003"	0.050 / 0.002"	0.030 / 0.001"
f). Line to Line Clearance	0.127 / 0.005"	0.100 / 0.004"	0.075 / 0.003"	0.050 / 0.002"	0.030 / 0.001"
g). Via Cover Dot Dia (on Plane)	0.381 / 0.015"	0.150 / 0.006"	0.127 / 0.005"	0.100 / 0.004"	0.050 / 0.002"
h). Line Width (on Plane)	0.200 / 0.008"	0.100 / 0.004"	0.075 / 0.003"	0.050 / 0.002"	0.030 / 0.001"
i). Clearance Dia.	0.990 / 0.039"	0.455 / 0.018"	0.280 / 0.011"	0.200 / 0.008"	0.110 / 0.0043"
j). Via Pitch (on Plane)	1.120 / 0.044"	0.560 / 0.022"	0.356 / 0.014"	0.254 / 0.010"	0.140 / 0.0055"

\* Target Value, Material is limited  
unit: mm / In

Table 1 Design Rule for Ceramics

The other direction the packaging industry developed is in the area of post metalization technology. The principal technology of choice was the use of thin film fabrication techniques. Thin films can be deposited either in a multilayer format using organic dielectric materials, such as polyimides, Fluoropolymers or BCB (bisbenzocyclobenzene). The conductor material can be copper, chrome, gold, aluminum and even exotic materials, such as Niobium. In the case of single layer thin films, material alloys as Titanium/Tungsten,

Titanium/Molybdenum are also used. This thin film processing can improve the geometry's another 40%, which brings the via diameters, lines and space to 30 microns with a pad pitch to less than 100 microns.

Although thin film technology is attractive from a design rule perspective, the cost associated with it has been very unattractive. This technology has been

### Microvia Technology

Another packaging technology, which supports and has even promoted the PCB packaging industry, is microvia technology. Currently, there as many as 20 different vendors and different technologies supporting the lower cost high density packaging market. The basic concept of this packaging construction is illustrated in the figure 1.

Figure 1

The fabrication of this class of packaging incorporates and starts with a core PCB board either composed of FR4, FR5, BT resin () or any other compatible core

material. Subsequent steps of coating epoxy resin materials, defining via holes and plating copper conductors either plated or etched to a patterned design. Depending on the vendor, the material and configuration of the structure, may deviate in the process. The conductors are normally constructed either through a subtractive, additive or semi-additive plating process. All processing can be patterned with via hole diameters; line and space geometries of 30 microns with pad pitches of 100 to 150 microns. Furthermore, the microvia built-up portion can be and is desired to be fabricated on both planes of the core board for mechanical stability. Illustrated in the figure 2 is a common fabrication process.

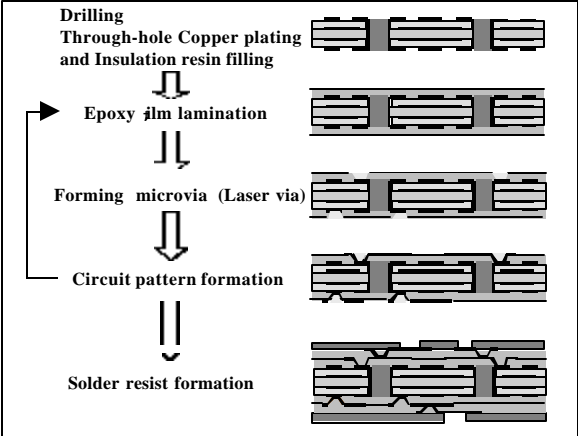


Figure 2

Microvia technology gives the designer the flexible to incorporate power and ground planes in core section of the construction, while putting fine line

transmission signals in the built-up portion.

Since organic materials are used, the electrical performance is typically superior for high digital signal propagation. The disadvantage is, of course, inferior dielectric properties for decoupling capacitance and high loss tangent delta numbers affecting high RF and digital frequencies. A comparison of the material characteristics is listed in table 2.

	Method	Material Characteristics		Value
		Item	Unit	
Thermal	TMA (Tensile)	Tg	deg.C	187
		CTE-P	ppm/K	89
		CTE-2	ppm/K	196
	DMA	Tg	deg.C	220
Decomposition	TG-DTA	1% Weight Loss	deg.C	294
Mechanical	Uniaxial Tensil	Break Strength	MPa	58.8
		Elongation	%	5.6
		Young's Modulus	MPa	2.14
Insulation	PCT	IR (between Layer)	ohm	>10 <sup>10</sup> (168H)
	HAST	IR (between Layer)	ohm	>10 <sup>10</sup> (168H)
Electrical	Dielectric Constant	e (1MHz)	-	3.9
		tan δ (1MHz)	-	0.031

Table 2

*Improved Dielectrics*

The mechanical features of high density packaging have been addressed; the need for superior electrical performance has also caused a need for superior materials exhibiting excellent dielectric properties. New classes of ceramic materials have been introduced to the market with mixed acceptance. Since propagation delay is directly proportional to the square root of the dielectric constant, ceramic manufacturers have centered their research on a class of materials referred to as LTCC (Low Temperature Cofired Ceramics). Listed in table 3 is a list of the well known industry LTCC materials with their corresponding material properties. These materials exhibit excellent dielectric properties with very low

dielectric loss characteristics. The conductor metal is also superior in its sheet resistance. Copper, Gold and Silver are the standard conductor metals

Integrated into the LTCC system. Probably the most important attribute of these technology is the integration of passive components.

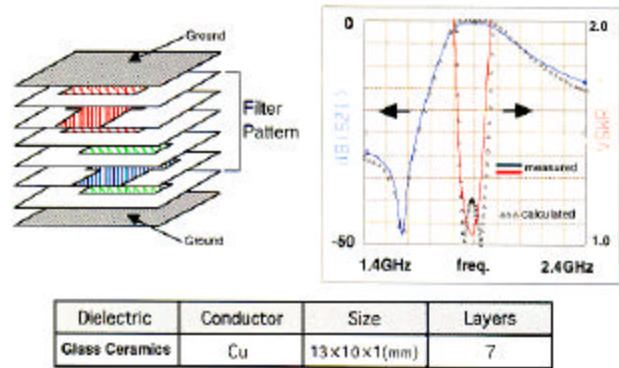


Figure 4

Property	G55*	GS1**	A6**	A473	AN242	GL660
Green Thickness	Various	AT - 0.0045 ± 7% AZ - 0.0060 ± 7% AX - 0.0075 ± 7%	AS - 0.005 ± 0.8%	Various	Various	Various
Fired Thickness	Various	AT - 0.0037 AS - 0.0055 AZ - 0.0083	AS - 0.0039	Various	Various	Various
XY Shrinkage (%)	15	12.7 ± 0.3	15.25 ± 0.15	15	19	18
Z Shrinkage (%)		15	22.825 ± 1.13			
Density (g/cm <sup>3</sup> )	2.8	3.1	2.5	3.6	3.4	
Flexural Strength (MPa)	200	320	210	314	400	200
Young's Modulus (GPa)	110	152	92	255	320	
CTE (ppm/°C)	5.5	5.8	7	6.9	4.7	6.2
Thermal Cond. (W/mK)	2.5	3.0	2.0	16.7	150	1.3
Dielectric Strength (kV/mm)	18	>40	20	10	18	
Conductor Resistivity (mΩ/sq)	3	3-9	<3	8-13	13	2-3
Print Definition (100µm mil)		4/4	4/4	3/3	4/4	
Via Material	Cu	AuAg + mixed	Au	W	W	Cu
Dielectric Constant (1.0GHz)	5.7	7.15	5.9 ± 0.15	8.8 See Next Pg	8.6	9.5
Dissipation Factor (1.0GHz)	0.0012	0.004 - 0.006	0.0012	0.0009	0.0053	.30
TGC (ppm/K)	71	+ 1386	+ 85	+ 117		

\* Currently Optimizing G55 for Higher Volume Production  
\*\* Demonstrated External to Kyocera



Table 3

Because noble and high conductivity metals are utilized with low dielectric constant materials higher "Q" values can be obtained. The fabrication of high speed digital and RF circuits can be designed with inductors, passive filters resonators and impedance matching circuits to fully exploit the insulator qualities of the materials. Depicted in the figure 4 is a seven layer filter design with its corresponding filter characteristics. In figure 5. Is a multilayer LTCC structure incorporated with integrated passive elements for a power amplifier application.

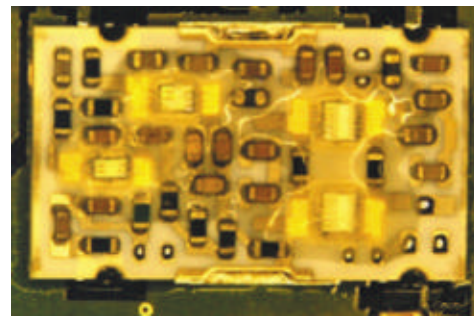


Figure 5- Power amplifier LTCC substrate

Now these embedded circuits have the features that can be tuned to improve the manufacturing of these high frequency application and eliminating costly tuning and assembly steps.

### Conclusion

With the increasing demand at the device level for finer geometry's and higher performance, packaging manufacturers are providing viable solutions. The materials ranges from HTCC to LTCC to organic platforms with design rules that meet device density and attachment requirements.

Packaging manufacturers today must continue to extend their current capabilities as well as invest in new technologies. Those packaging manufacturers that make and execute

those plans will remain as an enabler in the market place.