Transient Thermal Modeling Techniques for WBG Device Packaging

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Outline

- Introduction
- Thermophysical Material Characterization
- Finite Element Global/Submodel Methodology
- Results
- Conclusions
Who is Kyocera America?

Our San Diego facility is a major supplier of metallized ceramic packages for RF and microwave wireless telecom devices. Kyocera America offers a complete line of multilayer ceramic/organic packages for semiconductors in commercial and military markets. We also offer in-house flip-chip and wire-bond packaging services.
What is a Wide Band Gap (WBG) semiconductor?

- The definition is not very well defined but since a direct comparison of Si seems logical. It is usually taken as 2X the energy band gap of Silicon or approximately 2.0 eV.
- This includes Indium Nitride (InN) all the way up to diamond which is approximately 6.4 eV.
- GaAs is approx 1.4 eV and Si$_{1-x}$Ge$_x$ is approximately .7~1.1 eV.
- Some good online sources of info/data are:

  www.onr.navy.mil/sci_tech/31/312/ncsr/

  www.ecn.purdue.edu/WBG/
WBG Motivation & Thermal Management

- A large band gap translates to a high breakdown potential which allows the design of power devices that can operate at higher voltages and temperatures (i.e., higher power density).
- Silicon is frequency limited around $\geq 2.5$ GHz. By definition of their excellent electrical transport properties (small dielectric constant and high saturation velocity), WBG semiconductors allow for much higher frequency during operation.
- WBG semiconductor devices would reduce the number of Si based amplifiers in the wireless infrastructure world.
- WBG typically have better thermophysical properties also versus Si.
Recall this is a “transient” analysis discussion thus thermal energy transport is governed by the materials **thermal diffusivity**. Measures the ability of a material to conduct thermal energy relative to its ability to store.

\[
\alpha = \frac{k}{c_p \cdot \rho}
\]

**where:**
- \(\alpha\) = thermal diffusivity *(thermophysical prop)*
- \(k\) = thermal conductivity *(transport property)*
- \(c_p\) = specific heat capacity @ constant pressure *(thermodynamic property)*
- \(\rho\) = density *(thermodynamic property)*
  
  \([c_p \rho]\) = volumetric heat capacity

The performance of electronic systems degrade in proportion to the environment temperature. This temp also determines the service life of the electronic component. An industry rule-of-thumb at or near the design operating temperature states the \(N_{50}\) is cut in half for each 10C rise in temp. Excessive high temps can degrade the chemical/structural integrity of various semiconductor devices. Large fluctuations of temp as well as spatial variations of temp in equipment become responsible for most field failures.

**The purpose of thermal design is to limit spatial variations and maintain some nominal value.**
BeO, InP, and SiC thermal diffusivity is governed by typical nonconductor phonon transport mechanism (e.g. lattice vibration) and decrease rapidly with inverse of temperature.
Laser Flash System To Measure Thermal Diffusivity

Description: Custom apparatus measures *thru-plane* thermal conductivity (TC) of a material whose one side has been subjected to a short duration laser pulse. The resultant time vs. temp is monitored by an IR detector. Material TC is resolved by fitting the shape of this temperature rise curve to a 1-D heat flow model.

\[
\frac{\partial T}{\partial t} = \frac{\kappa}{\rho C_p} \times \frac{\partial^2 T}{\partial x^2}
\]

KAI Proprietary TC System used to validate thermal material properties used in package design (1999).
Closed-Form Solution vs. Simulation

Most thermal pkg design problems are 3D and irregular by nature which don’t lend themselves to transient closed-form solutions. The finite element method (FEM) provides us a robust numerical technique to solve these specialized cases.

ANSYS™ steady state thermal example

Typical Global Model Results cont.

*Validate even simple models!*
ANSYS™ FE Model File Description Hierarchy

Design variables parameterized for easy FE model changes.

ANSYS input file calls 2D IGES geometry file. Drawing areas are sub-divided for better mesh control.

Ansys text based input file example (*.in)
WBG Example: Bipolar RF Ceramic Package

Detailed view of \(\frac{1}{4}\) symmetric typical submodel solid model. Thermal bc’s specified on all surfaces except top face.
FE Submodel Technique for Increased T(t) Resolution

Submodel location

Course mesh global model with $\frac{1}{2}$ symmetric submodel volume outline shown in green.

heat gen volume

Detailed view of $\frac{1}{4}$ symmetric submodel. Thermal bc's specified on all surfaces except top face and symmetric planes.
Global model temperature plot after ten cycles with WCu heat sink

Transient Analysis Conditions:
200us pulse width @ 10% duty cycle
Bottom global model prescribed at 90C for this example, typically an effective convection coefficient is used ( W/mm²K).

Submodel temperature plot after ten cycles

WBG Bipolar RF Ceramic Package Results
Device is not operated in a continuous “on” state, a transient analysis must be conducted considering the time varying power pulse [e.g. P(t)].

We will define the “on-time” of the cycle to be when the output is high, and the “off-time” when the output is low. Duty-cycle is defined to be:

\[ \text{Duty-Cycle} = \frac{\text{On-Time}}{\text{On-Time} + \text{Off-Time}} \]

10% Duty Cycle Transient ΔT History.

Quasi-steady state sub-model max \(T_j=283°C\)

Quasi-steady state global max \(T_j=268°C\)

15 °C resolution due to submodel technique
Sharp “spike-like” thermal gradients can be resolved with submodel technique.
Key Concept: Most Temperature Rise in Device
ANSYS Model “Typical” Output

Key locations in FE global/submodel are tracked in the time domain

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Global Model Nodal Results

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Submodel Nodal Results
FE Submodel Technique Also Used for GaAs FETs

Course mesh global model with ½ symmetric submodel volume shaded. Note: constraint equations were used to tie h/s course mesh with GaAs fine mesh.

Detailed view of ½ symmetric submodel. Thermal bc’s specified on all surfaces except top face.
**AuSn Solder Die Attach Transient Thermal FE Results**

Very little capacitive thermal coupling between P/A stages (e.g. thermal diffusivity of all materials is high)

\[ \alpha = \frac{k}{\rho \cdot c_p} \]

- \( \alpha \) = thermal diffusivity
- \( k \) = thermal conductivity
- \( \rho c_p \) = volumetric heat capacity

Global Temp Plot During Pulse Off Conditions.

10% Duty Cycle Transient \( \Delta T \) History for all P/A Stages.
What if Scenario: Epoxy Die Attach

Transient $\Delta T$ History
(4mil epoxy @ $k=2.0$ W/mK)

Eventual quasi-steady state temperature achieved after $\approx 8$ sec

Monotonic sawtooth response due to poor thermal diffusion (i.e., low epoxy diffusivity)
Validation: KAI-R&D Internal $\theta_{jc}$ Measurements

Scope:

Conduct steady-state internal $\theta_{jc}$ measurements on laminate heat sink pkgs. The control group shall be a conventional CuW pkg in the same outline.

Fig. 1 (a) KAI-R&D infrared $\mu$thermal imaging system to measure package $\theta_{jc}$. (b) Detailed view of package measurement setup showing sample coated with a fine layer of high emissivity paint for a reliable IR scan (Note: Si is translucent at 5$\mu$m).
\( \theta_{jc} \) Measurement Setup Description

Fig 4: (a) Test setup with description. (b) A1670 package with thermal test die attached. (c) Kyocera 5 x 5 x .4mm 100W silicon thermal test chip dwg, illustrating RTD temperature sensor pattern and heater resistive pattern.
Steady State IR Measurement Results cont...

Average temperature for area was taken as $T_j$, refer to histogram bottom left.

Non-uniform heating of die face clearly visible.
Conclusions

- Thermal behavior of WBG devices can be effectively modeled using standard FE tools. Careful understanding of boundary conditions is critical.
- Must characterize thermophysical materials over temperature of interest.
- Should include device transistor details in thermal model. Majority of temperature rise is in top layers of device.
- Validate thermal model assumptions via IR imaging in time domain (TBD).
- Thermal design is one part of an integrated design approach.
Appendix
The thermal interface resistance across a joint is a complex function of the geometric and thermophysical properties of the contacting solids and of any interstitial substance at the interface (i.e., air or thermal grease). The important parameters are: surface texture, waviness, hardness, modulus of elasticity, mechanical load, temperature levels, and material conductivity's.

(refs: Incropera & Dewitt, M. M. Yovanovich - MHTL Waterloo)
Cooling Strategy Will Be Critical!

Typical phased array radar conduction path, note interface 2 and interface 3.


Example of liquid cooling of chip face